Accel-RF Instruments Corporation

High-Voltage Switching Device Testing

using the

AARTS HV System

AN #20140925-01

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1 Overview

The advanced development of new technologies, such as SiC and GaN, have created the opportunity for more efficient and higher voltage/power performance in switching and power management circuits. Their high cutoff frequencies, low on-state resistance, and very high breakdown voltages can increase power supply power handling densities approaching hundreds of watts/inch.

Reliability of these new technologies and techniques is critical for realizing practical applications. While Silicon devices have a rich history of proven reliability, these newer compound semiconductor technologies are too new to have a reliability history and have not been well proven. Further, process variations, even in well-controlled lines, yield widely varying results. This has driven the need for additional testing and to burn-in devices prior to delivery.

Accel-RF Instruments (ARF) has developed a test system capable of measuring reliability under a variety of conditions for switching power applications up to 1kV (off) and 25A (on) at a up to 1-MHz switching frequency (depending on high voltage level). By leveraging our existing RF burn-in tray platform, support for testing of multiple devices under elevated temperature stimulus in a small physical area is efficiently facilitated.

Reliability testing of switching power devices requires the balance of several competing challenges. The first is to understand the intrinsic reliability under application conditions without destroying the device as failures are induced. In order to properly analyze this, a “soft-switching” methodology is useful. In this approach a high-voltage signal is applied when the device is OFF, followed by a high current surge when the device is ON. In the OFF state there is very little current (leakage), and in the ON state there is very little voltage (assuming R_{ON} is small); hence, power dissipation in the device is minimized in either state. Using proprietary techniques, ARF has developed a test methodology that provides excellent separation between the high-voltage and high-current modes; thus providing the reliability engineer a well-controlled test regime.

A competing requirement for reliability evaluation is realizing a circuit that emulates a real-life application in what ARF refers to as “hard-switching” operation. In a real application, due to reactive loading, there is a small interval of time during each cycle in which high current and high voltage can exist at the same time in the device. For example in a 1-MHz switching regime (i.e. 500ns ON and 500ns OFF) there might be 1- to 10-ns in which high current and high voltage exist simultaneously. Depending on the duty factor of such a condition, this can significantly increase the power dissipation in a device. While this is very “application dependent”, it is nevertheless a reality, and can dramatically affect reliability.

The ARF power switching system includes provision for supporting real life hard-switching application circuit testing. In this case, the challenge is simulating a large “load” condition without having to dissipate that power locally. ARF has developed a technique using recirculating currents in which the device and load operate in tandem to emulate the full stress on the device under test (DUT) while only dissipating the power that would normally be residual in the application (i.e. a high-power load is not required).

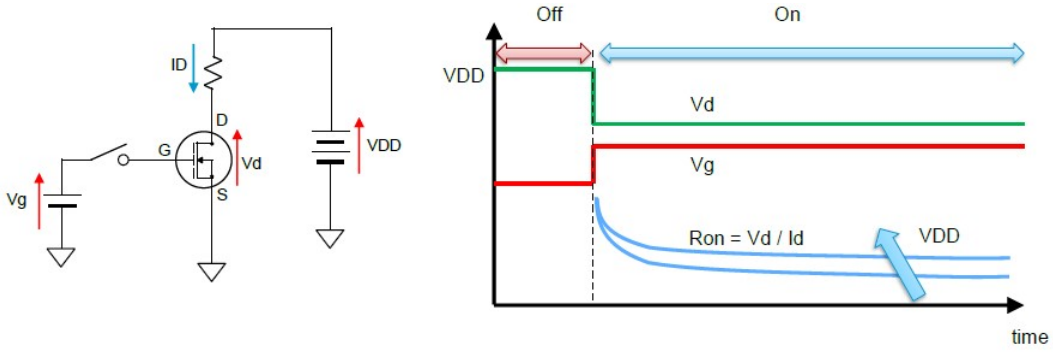
As is evident in either scenario accurate measurement of the instantaneous high-voltage and/or high-current values in the fast switching (up to 1-MHz) environment is highly desirable. Using small aperture track-and-hold techniques, the ARF system is capable of measuring synchronized instantaneous ON-state resistance and OFF-state leakage values obtained at user-defined points in the switching waveform.

Note: it is not practical to design a single board that supports both soft and hard switching options simultaneously. However, the base HV drawer may be easily configured with any mix of the modules of interest. Hence, ARF offers the soft- and hard-switching modules as separate optional products.

1.1 Current Collapse & Dynamic R_{ON}

R_{ON} is the drain-to-source resistance of the FET device in the ON state. Dynamic R_{ON} is the change in that resistance after the OFF-to-ON switching event. As illustrated in Figure 1-1, R_{ON} of GaN devices changes with time and is a function of OFF-state voltage. The higher the OFF-state drain voltage the less the resultant ON-state current when switched ON (i.e. R_{ON} increases); hence, the term current collapse.

Figure 1-1: Dynamic R_{ON} Change in GaN FET [1]



The change in R_{ON} is caused by electron traps that "resist" smooth current flow from drain to source. Once those electrons are removed (by drain-source current flow in the ON state), the channel resistance reaches its final low-value state. This time-dependent recovery is referred to as dynamic R_{ON}. The traps are generated by the high-voltage from drain to source during the OFF state. This effect obviously affects device power dissipation, and ultimately usefulness.

Two factors significantly affect transistor performance. R_{ON} defines the steady-state power dissipation (i^2R), and gate charge Q_G affects the switching performance of the device (e.g. the rate at which the device can be turned ON and OFF) and ultimately the requirements of the gate drive circuitry. These factors are inversely proportional, meaning a device design that yields a lower gate charge yields higher R_{ON}, and vice versa. Hence, a common "figure of merit" for transistors operating in this mode is $R_{ON} \times Q_G$, which can also be thought of as a measure of switching efficiency.

A comparison of several devices and technologies is presented in Figure 1-2. As can be seen GaN devices do not offer as high breakdown voltage performance as SiC, or even some Si devices; but, they do offer much better switching efficiency at voltages up to 600 V.

In real power supply applications the device is generally switched from ON to OFF at a rate between a few kHz to tens of MHz. The higher switching frequency yields smaller support components (especially inductors). The problem GaN currently suffers is that R_{ON} varies with time following the transition from OFF to ON (i.e. dynamic R_{ON} as described above). As can be seen in the plot of Figure 1-3, the residual drain current is sweeping out the traps during the 10-μs interval shown. Clearly during that time, the higher R_{ON} results in undesirable power dissipation. The plot on the right illustrates the desired performance. Figure 1-4 shows an expanded view, indicating it has not yet fully recovered (de-trapped) even after 100μs.

Figure 1-2: R_{ON} x Q_G Figure of Merit Comparison [2]

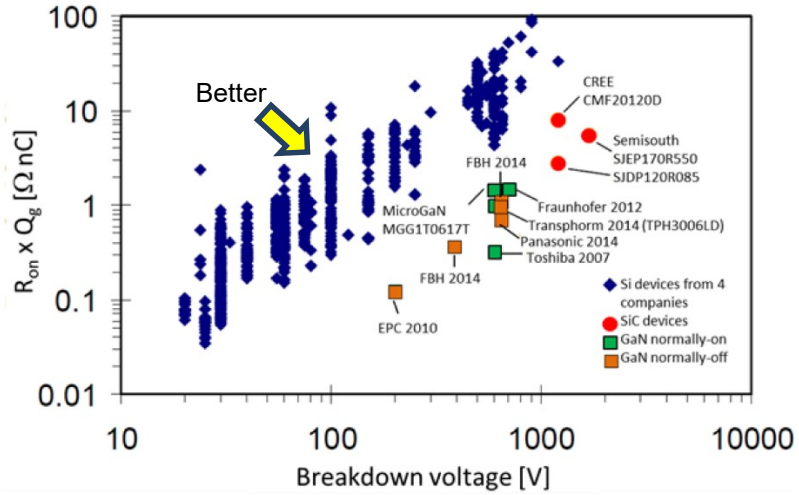


Figure 1-3: Dynamic R_{ON} Switching Transients [2]

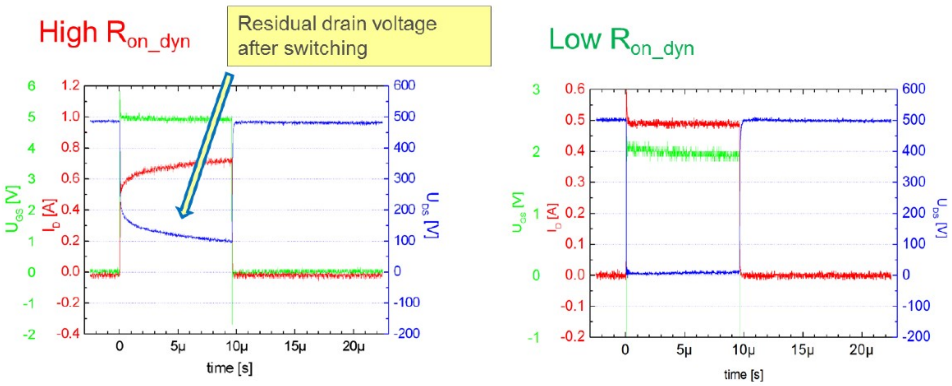
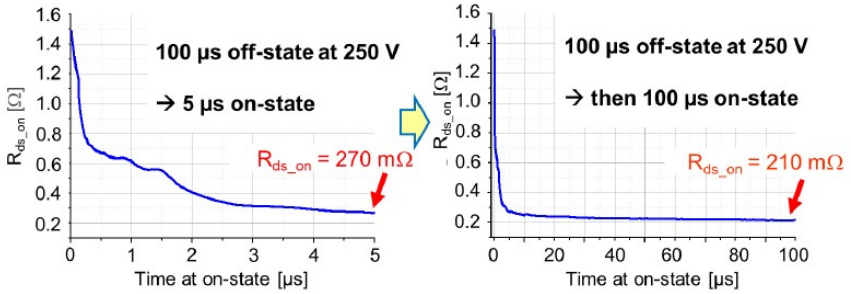
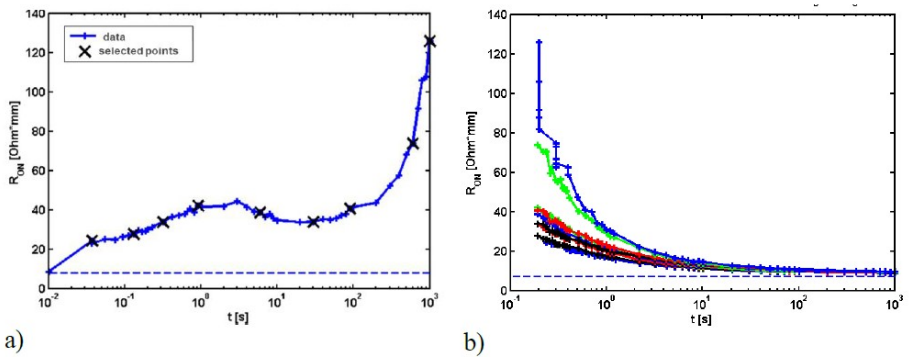


Figure 1-4: Detrapping Event (R_{ON} vs. Time) [2]



Another interesting phenomenon is that the amount of traps is very dependent on the time the device is held in the OFF state. Figure 1-5 shows that for very long OFF states (1000 s in the plot) R_{ON} continues to increase due to the additional traps generated. Each point in the left plot shows R_{ON} as measured at 200 ms after the switch to ON event. The right plot shows the longer-term time dependency of the de-trapping process.

Figure 1-5: Dependence of R_{ON} vs. Time for Various OFF-State Time [2]

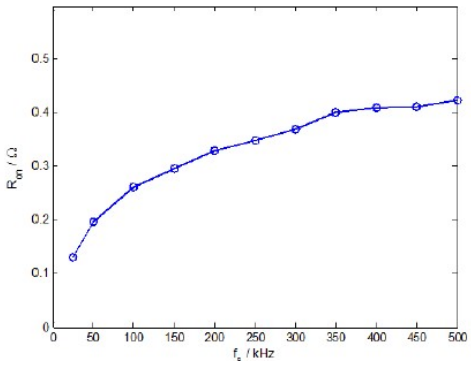


Dependency of dynamic R_{ON} duration induced by duration of off-state bias at 200V prior to switching event.

Time dependency of de-trapping at V_{DS} = 1V and V_{GS} = 1V after OFF-state biasing according to the data points selected in 1.

Perhaps the most important effect that drives system design of the ARF HV test systems is shown in Figure 1-6. The horizontal axis is switching frequency, and the vertical axis is R_{ON} (measured at 250 ms after pulsing stops). It may be observed that dynamic R_{ON} is 8x higher than the static R_{ON}, and represents the average traps (driven by the relative ON and OFF state trapping and de-trapping time constants). What this shows is the importance of measuring R_{ON} at real operational switching rates.

Figure 1-6: Dependence of R_{ON} vs. Switching Frequency [2]



The maximum realistic hold off voltage for 10-MHz switching rate is currently ~200 V, and for 1-MHz rate is ~600 V. Otherwise, the devices would burn themselves up. This has nothing (yet) to do with the dynamic switching reactive power dissipation that occurs during the edge transitions of the switching events themselves, as experienced in a real application.

1.2 Failure Mode Evaluation Options

As illustrated in Figure 1-7 there are three primary regions of operation in a typical switching application: ON state, OFF state, and the in-between dynamic transition state. Note that the red trace illustrates what can happen in a real application. There is a region in which high voltage and high current exist simultaneously, and hence power is dissipated during that time. This operation is sometimes referred to as "hard" switching. Since this operating mode represents what happens in the real application it is imperative that it be performed as part of the device qualification. However, from a practical perspective it can be very challenging to preserve the failing part for failure analysis as thermal runaway can happen very rapidly.

The blue trace represents what happens in a "soft" switching operation. In this case the test system performs the task of isolating the voltage and current from the transition event; hence, very little power dissipation exists. This is particularly useful for evaluating failure modes at the end points. Since the power dissipation is very limited and controlled, the problem of preserving the part for failure analysis is mitigated. Hence, it is useful for precisely evaluating intrinsic reliability.

Each of these regions may exhibit unique failure mechanisms. Further, one region (in particular the transition region) may significantly affect the failure mechanisms at the other regions as note by Joh[3] and Wurfl[2]. To provide maximum testing flexibility it is desirable to support both hard- and soft-switching options. However, with typical "application like" test setups it is difficult, if not impossible, to de-embed the dynamic transition modes from the ON- and OFF-mode effects. Even worse, many test configurations are only capable of generating a fixed or very limited range of pulse widths due to limited capacitor discharge characteristics. The ARF test setup offers a large range of stimulus options. The blue trace (i.e. HVSOFT operation) illustrates the most ideal situation for evaluating ON/OFF degradation mechanisms. The ARF HVSOFT module design supports soft switching options.

Figure 1-7: Hard and Soft Switching [3]

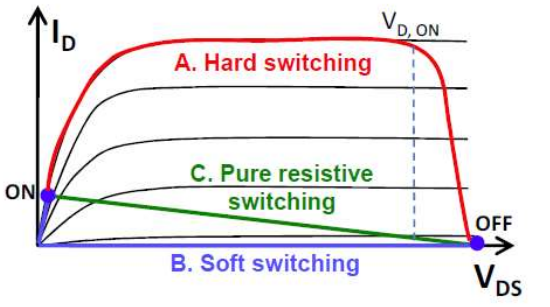
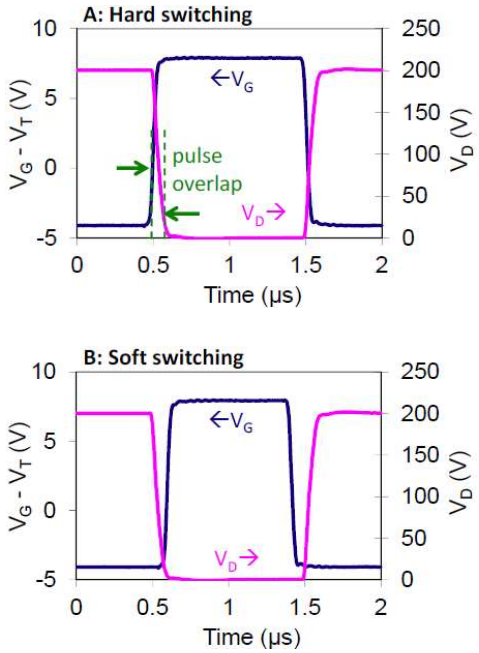


Fig 1. Various loadlines through which a power device switches between ON- and OFF-state: hard switching (A), soft switching (B), and resistive switching (C) loadlines. $V_{D,ON}$ is defined as the drain voltage at which the device is fully turned ON. Detailed waveforms are shown in Fig 2.



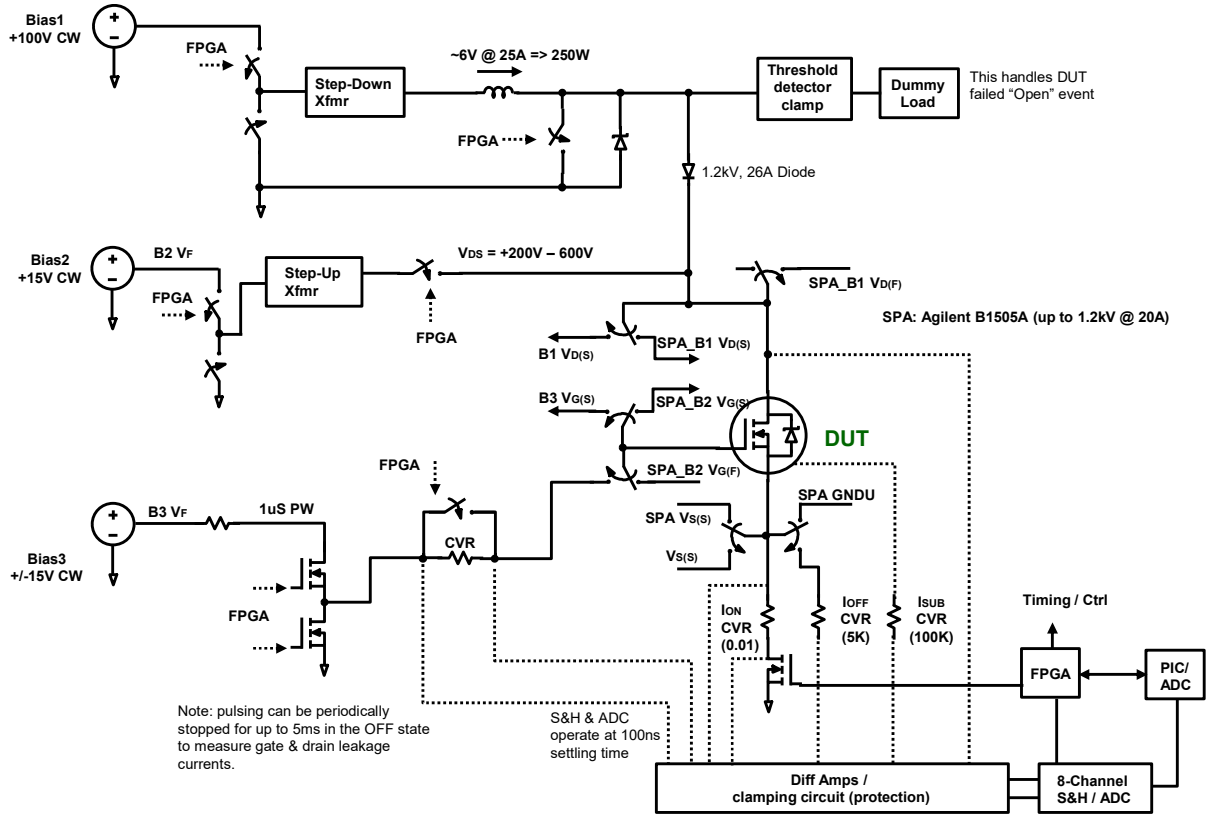
The ARF HVHARD module design supports “application like” product qualification testing, but at the expense of flexibility for selecting various pulse width and PRF options. The design techniques for the optional HVSOFT and HVHARD modules are described in more detail below.

2 Soft-Switching Module Design

In the ARF AARTS system, the concept of "soft-switching" implies avoidance of the condition in which high-voltage and high-current may exist simultaneously. As noted earlier, this can result is excessive power dissipation, which in turn can lead to extremely fast device destruction in a time frame for which it is impossible to protect – after which failure analysis is not available. A block diagram of the High-Voltage Soft-Switching Module (HVSOFT) is presented in Figure 2-1, with a picture of the actual unit shown in Figure 2-2. The HVSOFT module handles all of the dynamic switching between the high-current and high-voltage modes, including the charging and discharging of the device capacitance. Thus the device leakage current at high voltage and ON resistance at high current may be measured without residual thermal effects that would exist were the device to do the switching.

As shown in the block diagram, three supplies create all of the stimulus requirements. The HVSOFT design leverages an ARF custom triple power supply (a.k.a. Power Control Unit – PCU) that provides key operational features important for reliability testing; such as, fast shutdown upon over-current or over-voltage operation, supply sequencing, high-power Bias1 for drain sourcing, enhanced accuracy for gate current measurements, 4-quadrant operation for Bias2 and Bias3, etc…

Figure 2-1: High-Voltage Soft-Switching (HVSOFT) Block Diagram

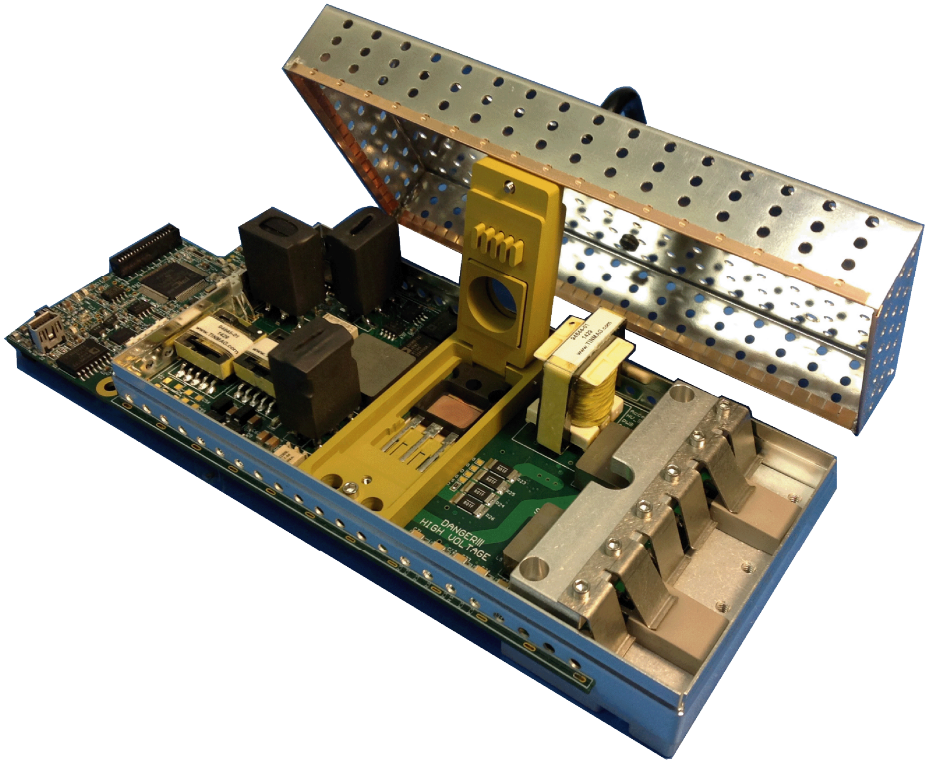


The high-power Bias1 provides the necessary source for the High-Current (HC) section. The 25-A capability requires up to 250 Watts to overcome circuit losses, and device drain-source resistances exceeding 100mΩ. A step-down transformer converts high voltage into high current to avoid routing large currents through the system. An innovative custom circuit design protects the module against a DUT-failed-open condition and damage due to the high-voltage connected in parallel with the high-current electronics.

A Bias2 4-quadrant supply provides the source for the High-Voltage (HV) section. It is intentionally current limited to minimize the energy available to the DUT. This protects the device from destruction upon a failure event, and provides some safety against accidental human contact. The step-up transformer creates ~100V to >1kV for 0 to 15V input. ARF has developed a high-voltage switch that minimizes overshoot in both the turn-ON and turn-OFF waveforms while simultaneously minimizing residual current requirement of pulsing capacitive loads using a proprietary energy recovery technique.

The Bias3 4-quadrant bipolar supply sources the gate pulsing circuit. Its ±15V capability supports testing of enhancement- or depletion-mode devices. As with all other parts of the HVSOFT circuitry, the gate control employs fast-acting protection against device drain-to-gate shorts (since a kV signal applied to low-voltage electronics can be destructive).

Figure 2-2: HVSOFT Module



R_{ON} is a key performance metric for power-switching devices. Simultaneous measurement of drain-to-source current and voltage are required to determine this value. A 6-channel synchronous ADC with Track & Hold (T&H) capability supports capturing a snapshot of those parameters (including drain-to-source voltage, drain current, and gate voltage) within ~100ns aperture window during the device "On" state. The timing of the aperture window is programmable with a 10-ns resolution. A second 6-

channel ADC captures the data in the corresponding "Off" state. This is useful for measuring OFF-state voltage and leakage currents.

Finally, trip circuits are employed to rapidly remove stimulus should a failure condition be detected for V_{GS}, I_{GS}, V_{DS}, or I_{DS}. within ~200nS. These trip functions are gated such that the user may define when the trip detection occurs within the pulsing waveform.

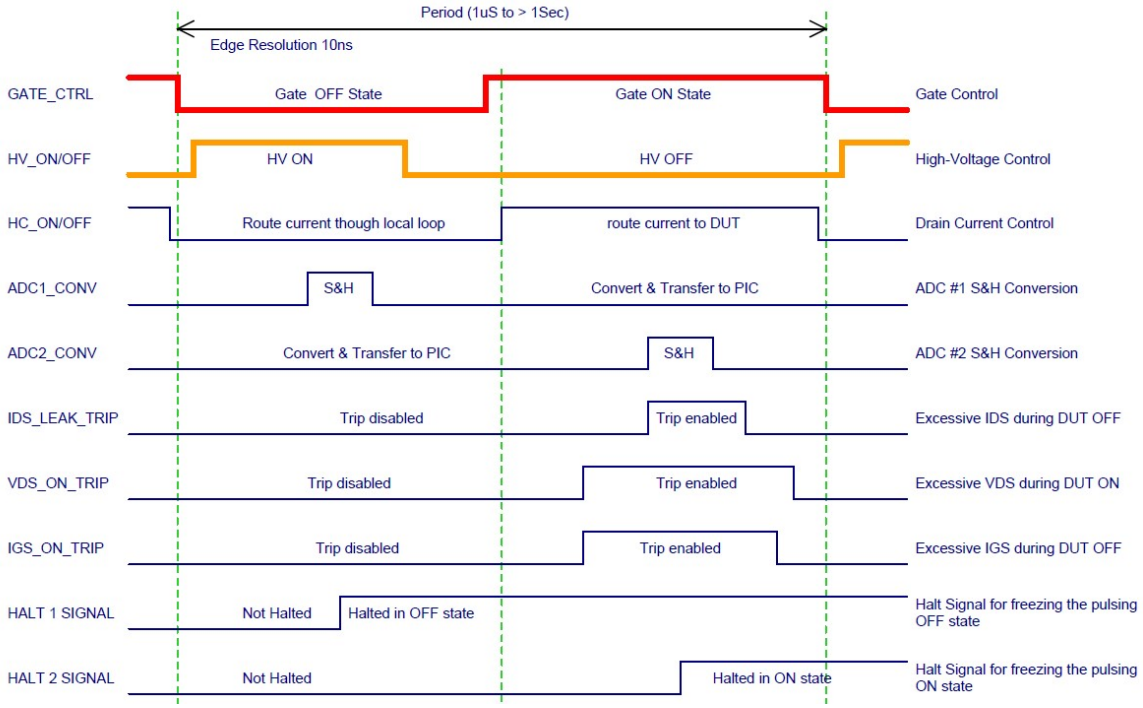
ARF's innovative design offers significant flexibility for controlling the waveform timing. All control signals are generated using an on-board FPGA, with a user-defined time resolution of 10ns. Pulse periods as low as 1μS (i.e. PRF up to 1 MHz, depending on the high voltage value) to in excess of 2 seconds are supported. CW stimulus may be applied as well. Note: PRF is limited by the following equation: PRF <= 7.2e9 / $(HV)^2$ Hz.

An example of the control signals is shown in Figure 2-3. Note that the HV and HC control signals are defined such that there is no overlap. All edges may be user-defined in a setup process using ARF's LifeTest or USBControl programs.

The user may also define when the ADCs are triggered for conversions. Hence, measurements may be made anywhere along the pulse waveform. The only requirement is that the signals must be stable during the preceding T&H aperture window of ~100ns.

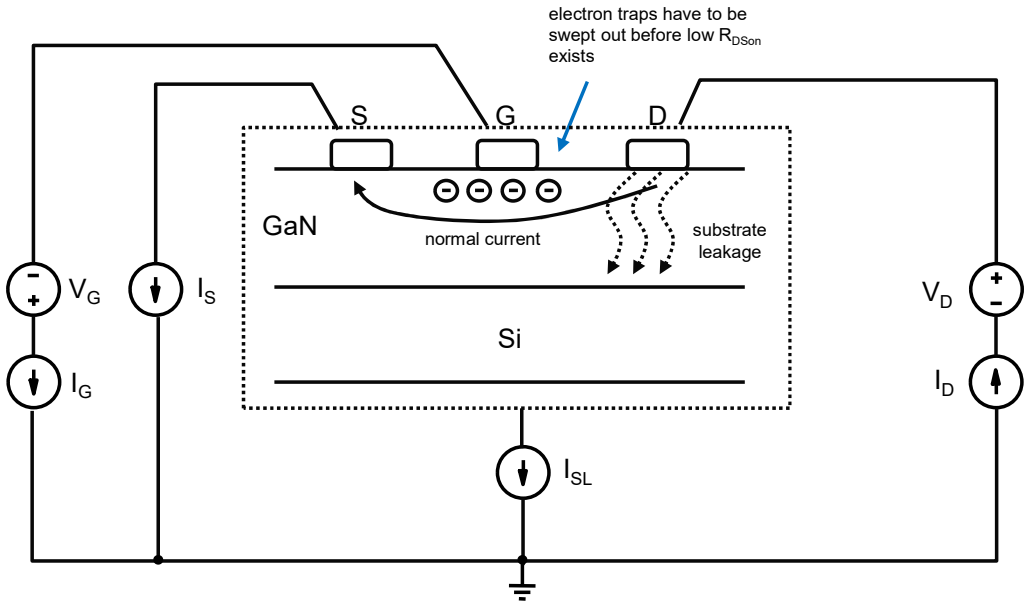
One problem exists when measuring very low currents (e.g. gate- and drain-leakage currents). The device capacitance must be charged through the local Current Viewing Resistors (CVRs). Yet, in order to generate a voltage large enough to offer reasonable resolution, those CVRs must be high in value (e.g. ~100kΩ). Hence, the RC time constant can be long (as compared to a 1μS period). For this reason, the software supports the capability to "Halt" the waveform at any point along the Period count (as shown in the waveform diagram). This facilitates accurate measurement the leakage values periodically for subsequent use as failure criteria.

Figure 2-3: Example Soft-Switching Waveform Timing



The standard HVSOFT board design provides an option (via mounting the device in a TO247-5 package) to remotely sense the source voltage, and to connect a substrate pin for measurement of substrate leakage. In some device structures substrate leakage is often the first indication of wear-out failure mechanisms. Figure 2-4 illustrates the system connections for measuring substrate leakage.

Figure 2-4: Substrate Leakage Measurement



Relays are provided at strategic points that support connection of an external Semiconductor Parameter Analyzer (SPA) (or other equipment for independent device characterization or confirmation) to any selected device. For instance, the Agilent B1505A supports a mode of operation for measuring the current collapse phenomenon by measuring RON vs. time after a specified application of high-voltage reverse bias in an OFF state.

Finally, the HVSOFT module employs a MUX system through which buffered versions of the key signals may be routed to an external oscilloscope. This may be used to verify waveform timing integrity of the selected device during the stress test interval. A separate trigger signal leaves room for two independent selectable measurements to be observed simultaneously.

2.1 HVSOFT Performance

The ARF HVSOFT module comprises a high-voltage section, high-current section, gate-drive buffer, and associated buffers/ADCs to stimulate and measure device performance over time. The OFF-state voltage is user programmable from ~100V to over 1kV. The ON-state current is ~1A to 25A. The gate drive circuitry supports +/-15V operation.

The ARF LifeTest program is designed to manage electrical and thermal stimulus, capture and store data, and analyze the results of that data over a user-definable measurement time. The system is designed to run continuously at full ratings.

In order to better understand the performance of the HVSOFT design, a test device Cree (Wolfspeed) C2M0025129D SiC MOSFET was employed as a test device. Its specifications are presented in Figure 2-5. The test stimulus is presented in Table 2-1. Figure 2-6 through Figure 2-8 show the

stability data of this device over time for the parameters of R_{ON}, I_{DSON}, and V_{DSOFF}, respectively. Note that the device was not being controlled thermally, and the performance has a slight tracking of room temperature variation. Even so, the data is quite stable.

Figure 2-5: C2M0025129D SiC MOSFET Performance Specifications

CREE

Electrical Characteristics (T_c = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	4	V	V_{DS} = V_{GS}, I_D = 15mA	Fig. 11
			2.1		V	V_{DS} = V_{GS}, I_D = 15mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			600	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	mΩ	V_{GS} = 20 V, I_D = 50 A	Fig. 4,5,6
			43			V_{GS} = 20 V, I_D = 50 A, T_J = 150 °C	
g_{fs}	Transconductance		23.6		S	V_{DS}= 20 V, I_{DS}= 50 A	Fig. 7
			21.7			V_{DS}= 20 V, I_{DS}= 50 A, T_J = 150 °C	
C_{iss}	Input Capacitance		2788		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		220				
C_{rss}	Reverse Transfer Capacitance		15				
E_{oss}	C_{oss} Stored Energy		121		µJ		Fig 16
E_{AS}	Avalanche Energy, Single Pluse		3.5		J	I_D = 50A, V_{DD} = 50V	Fig. 29
E_{ON}	Turn-On Switching Energy		1.4		mJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω,L= 412 µH	Fig. 25
E_{OFF}	Turn Off Switching Energy		0.3				
$t_{d(on)}$	Turn-On Delay Time		14		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 16 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		32				
$t_{d(off)}$	Turn-Off Delay Time		29				
t_f	Fall Time		28				
$R_{G(int)}$	Internal Gate Resistance		1.1		Ω	f = 1 MHz, V_{AC} = 25 mV, ESR of C_{ISS}	
Q_{gs}	Gate to Source Charge		46		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 50 A Per IEC60747-8-4 pg 83	Fig. 12
Q_{gd}	Gate to Drain Charge		50				
Q_g	Total Gate Charge		161				

Table 2-1: Cree SiC DUT Test Stimulus

Test Stimulus	
HV PW =	10µs
HC PW =	30µs
Period =	500µs
VGate =	15V
Vdrain =	600V
Idrain =	20A

Figure 2-6: R_{ON} Stability Data

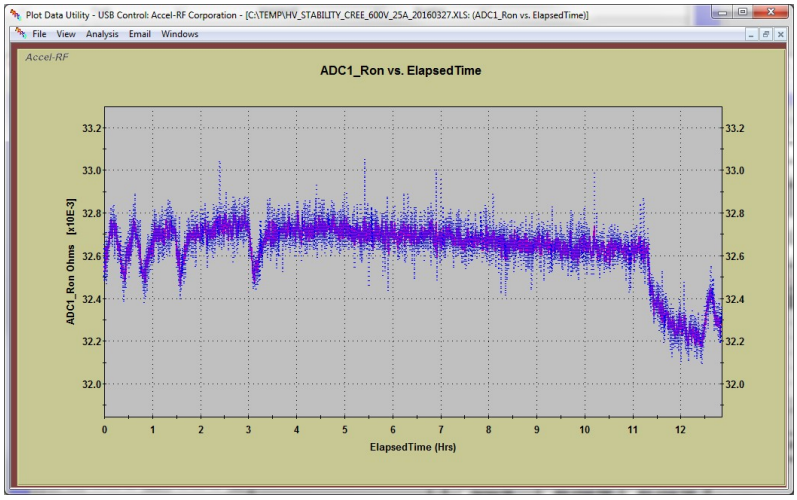


Figure 2-7: $I_{DS(ON)}$ Stability Data

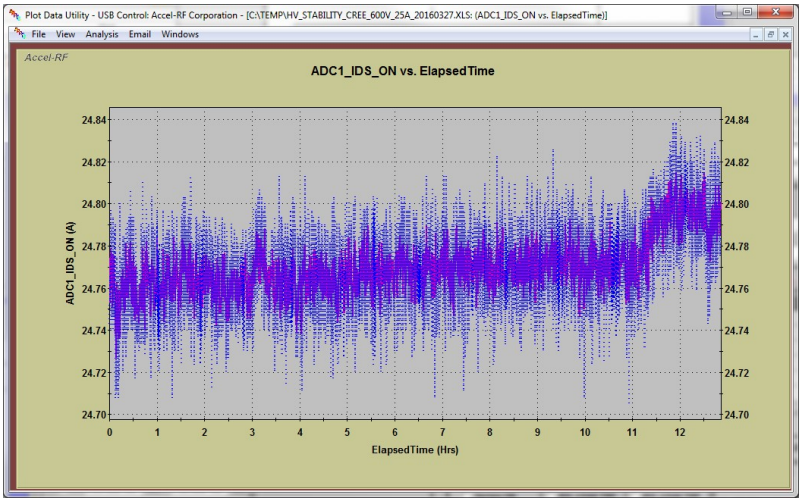


Figure 2-8: $V_{DS(OFF)}$ Stability Data

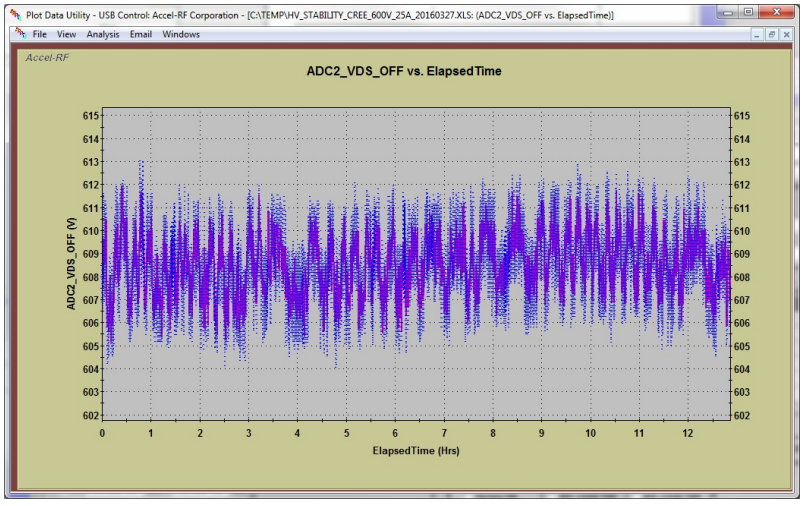
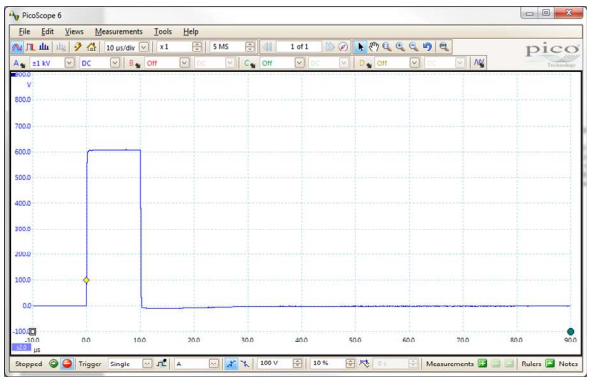
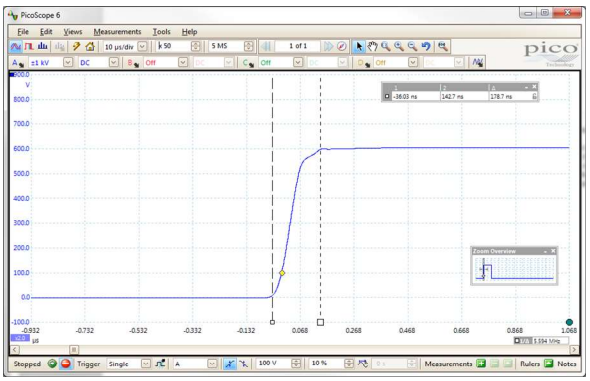


Figure 2-9 and Figure 2-10 illustrate the high-voltage pulsed waveform performance. To simulate a DUT OFF-State and associated pulse integrity when played against the expected worst-case DUT C_{DS}, a special test device containing shunt capacitance and simulated leakage resistance was employed. As can be seen, the pulse integrity is quite good. Further, due to resonant switching techniques, the energy required to charge the DUT capacitance is recovered during the discharge cycle.

Figure 2-9: 600V 20-uS Pulse



Rise Time = ~175ns



FallTime = ~130ns

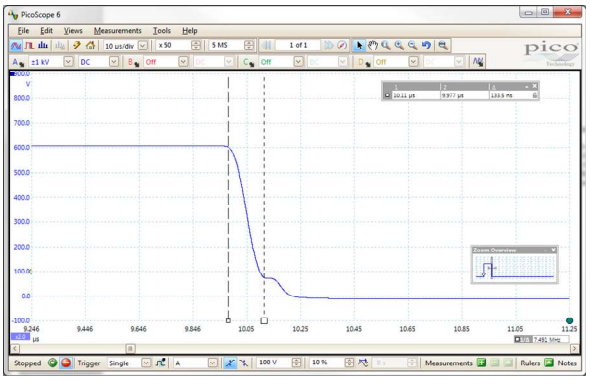


Figure 2-10: 600V 1-uS Pulse

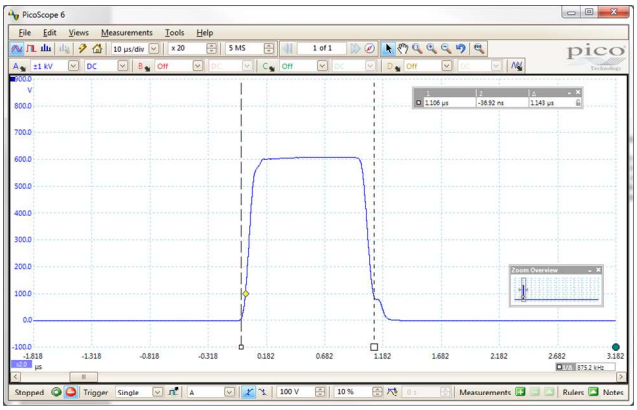
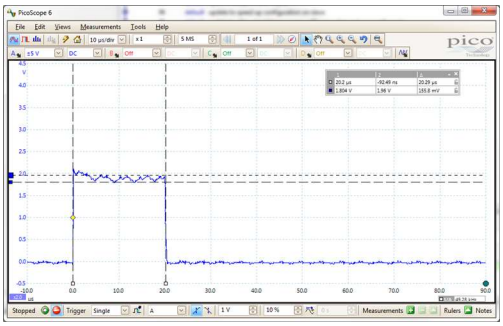


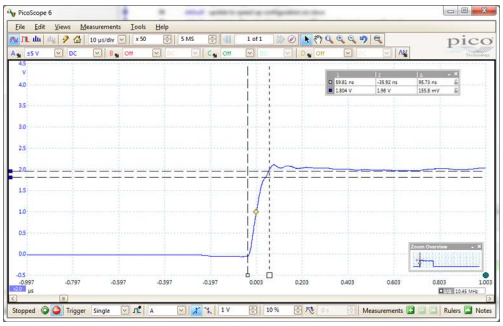
Figure 2-11 and Figure 2-12 present the high-current ON-state pulsed performance. In these cases, a simulated DUT using 0.1-Ω high-power load resistance from drain to source was employed. This allows measurement of current ripple by viewing the V_{DSON} voltage waveform as shown.

Figure 2-11: 20A 20-uS Pulse

~0.8A ripple



Rise Time = ~100ns



FallTime = ~500ns

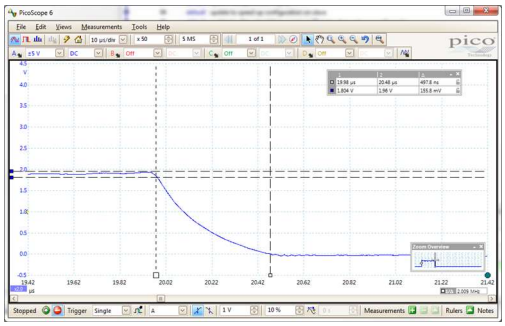
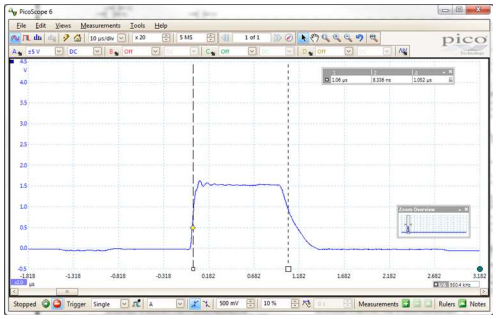
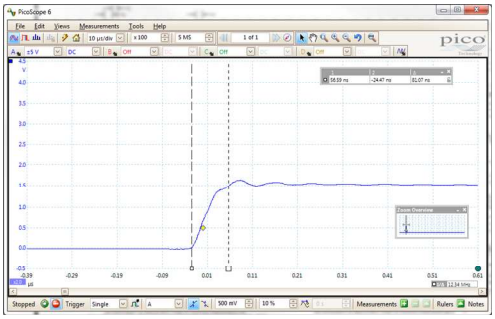


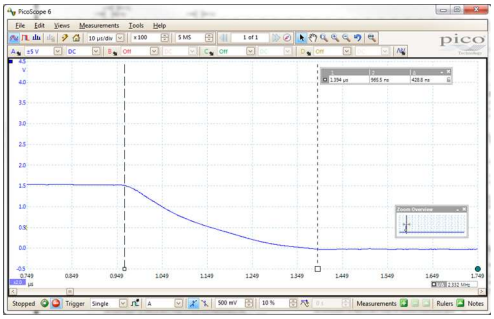
Figure 2-12: 15A 1-uS Pulse



Rise Time = ~110ns



FallTime = ~650ns

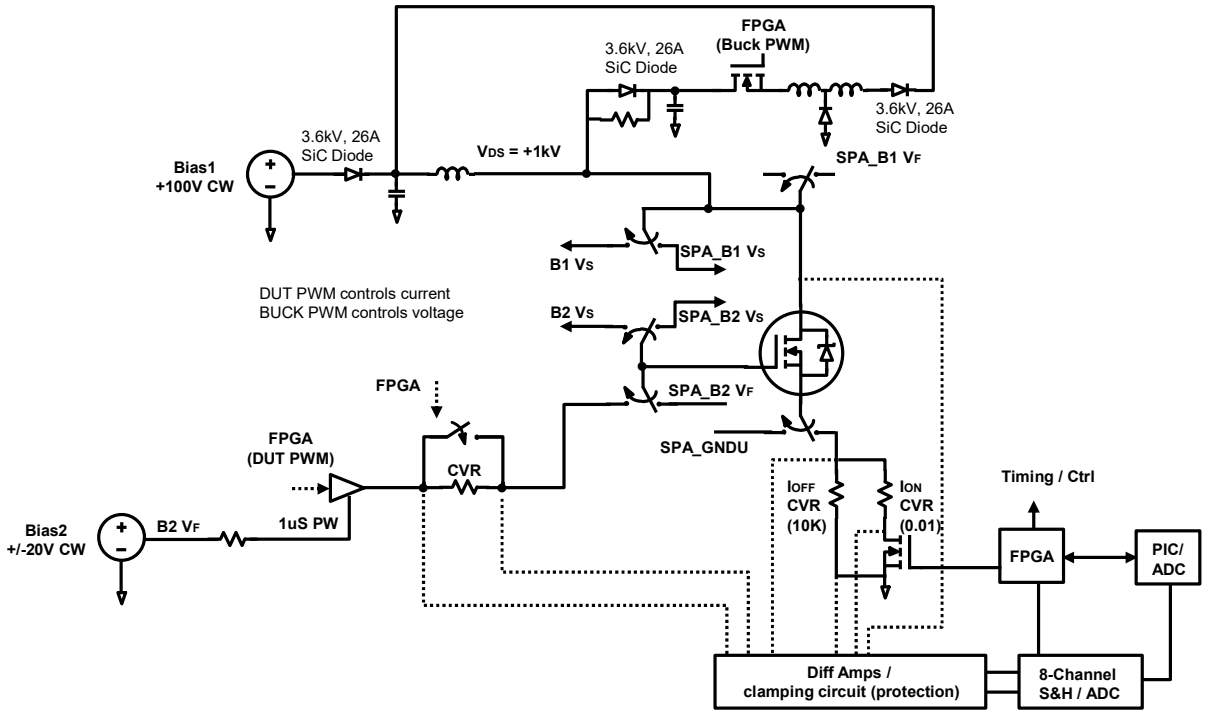


3 Hard-Switching Module Design

In the ARF AARTS system, the concept of "hard-switching" implies the implementation of circuit operation more consistent with a real application. While this can result in higher power dissipations, it nonetheless represents a more realistic operational stress condition. The soft-switching paradigm is more appropriate for the initial measurement and characterization of intrinsic reliability; whereas, the hard-switching paradigm would be more beneficial for final characterization prior to system deployment. The amount of stress induced by hard-switching is very dependent on circuit implementation, the amount of parasitic reactance, and load characteristics.

One difficulty in measuring "real" circuits resides in the fact that a large load is often required to simulate actual operation. This presents a challenge to the test set designer, particularly when many channels are to be tested. ARF has mitigated this problem by using a recirculating current approach. A block diagram of the High-Voltage Hard-Switching Module (HVHARD) is presented in Figure 3-1.

Figure 3-1: High-Voltage Hard-Switching (HVHARD) Block Diagram



In this innovative approach, the power that would normally be delivered to the load is routed back to the input for sourcing the power required for the next cycle. The diode, inductors, and capacitor in the upper section of Figure 3-1, combined with the buck regulator, act as a simulated "load" for the device circuit operation. It employs a resonance trick to "recover" the power delivered to the load and recirculate it back to the device input for the next cycle.

In a test system that does not employ current recirculation and a real "load" is employed, the source power must match the power delivered to the load plus residual losses, and it must extract the resultant heat. When working with KWatts of power that can be a significant challenge. Again, employing the ARF approach, the output power is "captured" and re-routed back to the input for the next cycle; thus, greatly reducing the facilities power and heat dissipation requirements.

Judicious selection of the feedback configuration emulates the stressful condition of the overlap of current and voltage at the device terminals, as would exist in a real application. Another convenient, yet significant, advantage of this approach is that the input Bias1 supply need only source enough power to overcome the residual circuit loss and the losses incurred by the DUT. It need not provide the power required to be delivered and dissipated in an actual load. This minimizes the facilities power require to the system.

One disadvantage of this hard-switching paradigm is that it must always be pulsing, and the feedback elements are chosen to match a fixed PRF. Hence, it is less flexible than the soft-switching design, which allows the option of stimulating the device in a static ON (high-current) or OFF (high-voltage) mode of operation.

4 Rack Design

The AARTS Power-Switching system leverages the same rack concept and motherboard utilized in the ARF RF Burn-In system. As shown in Figure 4-1, the tray fits in a standard 19-inch rack. A single 3U tray supports up to 8 DUTs. Multiple trays may be populated per rack to minimize space requirements.

Figure 4-1: Rack Tray Setup

The hard- and/or soft-switching modules are mounted in the tray as shown in Figure 4-2 (for an 8-channel configuration). In this case two DUTs share a common heater block, designed to heat only the device, keeping the high-voltage/current electronics cool. The modules are designed to be operated on a bench setup and the clamping mechanism offers a clearance hole for characterization under a thermal-measurement system (e.g. evaluating junction/channel temperature). The module may be controlled remotely via a stand-alone software tools provided by ARF.

Figure 4-2: 8-Channel Configuration

5 Summary

As new device technologies mature, it is important to verify device reliability before deployment in new terrestrial- and/or space-based systems. It is challenging to obtain standard device degradation data when operating in a powered pulsing application. The speed at which catastrophic failure occurs implies it is often impossible to assure the same failure mechanism has occurred, which is imperative for reliability calculations.

This application note has presented two approaches for testing high-power switching devices. The first (soft-switching) approach allows maximum flexibility for setting up numerous test scenarios: a range of PRFs from 1 MHz to <1 Hz (dependent on high voltage value); static ON or OFF testing; explicit control of current- and voltage-stimulus within the period time frame; fine control of ADC measurement sample times; and wide range of stimulus control (e.g. voltage- and current-levels). Most importantly, this approach avoids the mechanism by which rapid destruction occurs. Hence, intrinsic reliability is more easily determined.

The second (hard-switching) approach offers the advantage of emulating real-world operation without driving a need for many high-power loads or multiple high-power sources. As noted earlier, the circuit design is targeted for a specific mode of operation (e.g. fixed PRF), and must always be pulsing – application of static levels is not possible. This mode would be more appropriate as the final verification of a device for a specific application as it emulates the more stressful real operating mode.

The ARF power switching test platform supports flexibility to test a mixture of soft- and hard-switching modules. By leveraging the integration of its burn-in platform with new fast-switching measurement techniques, ARF offers the most flexible and accurate power switching platform available. It minimizes test set footprint, as well as facilities requirements (e.g. AC mains current).

ARF offers design services to customize the HVSOFT and HVHARD designs as needed. Please contact our San Diego office for more information.

6 References

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[2] J. Würfl, M. Troppenz, O. Hilt, E.Bahat-Treidel, N. Badawi, J. Böcker, S. Dieckerhoff; "*Dynamics of drift effects in GaN power switching transistors*", Personal Communication, 2015

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