White Paper

"Gallium-Nitride Solid-State Power Amplifier Reliability Analysis Report"

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1.0 Introduction

Over the past several years many research groups have been developing new compound semiconductor materials that have the potential to achieve very high levels of current density and power density per unit area. The most promising materials to date are Silicon-Carbide (SiC) and Gallium-Nitride (GaN). Semiconductor transistors manufactured from these materials open opportunities for major advances in RF power amplifiers [1].

One projected application of GaN based semiconductors is in the development of 30 GHz (Ka-Band) solid-state power amplifiers (GaN SSPA). GaN based semiconductors have demonstrated very high levels of RF power densities with high efficiency at these frequencies [2]. The next stage of development involves the realization of large area devices capable of reliably delivering RF power levels sufficient to enable the next evolution of phased-array antennas and compact high power transmitters.

The following report contrasts the predicted reliability for three different architectures of Gallium-Nitride based solid-state power amplifiers. Each SSPA architecture was designed to achieve 120 watts of RF output power at Ka-Band (31 to 36 GHz) using various methods of power combining multiple GaN transistors. Detailed information about the SSPA architectures can be found in JPL Report CL#04-1721, "Ka-Band Wide-Bandgap Solid-State Power Amplifier Task" dated September 1, 2004.

The goal of this work was not to predict the "absolute" reliability of the GaN SSPA architecture but rather to contrast the relative reliability between the three designs. Specifically, the absolute reliability prediction would be pre-mature at this date due to the fact that no GaN device exist that can deliver the high output power required. However, by applying some generic assumptions about the environment and using projected failure rates of the anticipated GaN device technology, a "relative" reliability prediction can be calculated. As long as all assumptions apply consistently between the architectures, a conclusion may be determined about which architecture would be the most reliable and what level of reliability-assurance tradeoff exists between the three architectures.

2.0 Review of Basic Definitions and Tools

(See Appendix A for additional information related to reliability prediction models)

2.1 Definitions:

MTTF : The mean time to failure (MTTF) is defined as the measured operating time of a single piece of equipment divided by the total number of failures of the equipment. It is also used to describe the mean life of a group of devices failing without replacement. MTTF varies as a function of time, which is difficult to handle in probability prediction models. Therefore, when determined from life test data it is common to determine an average MTTF proportional to the median-life time (i.e. time at which 50% failures occur). $MTTF_{ave} = t_{50}\exp(\sigma^2/2)$

FIT : The failure rate unit. FIT stands for one failure in 10^9 hours.

λ : Failure Rate. It is usually given in KFIT = KiloFits, with 1 KFIT standing for one failure at 10^6 hours. Like MTTF, λ varies as a function of time. When using life test data, a common approximation for λ_{ave} is $1/MTTF_{ave}$.

π factor : Failure Rate modifier. These are used in the MIL–HDBK–217F models to account for a variety of variables that affect failure rates, such as the operating environment, etc. The base failure rate is usually multiplied by the π factor to yield a more accurate prediction of MTTF under use-conditions.

2.2 Tools:

MIL-HDBK-217F is the guidebook for calculating a failure-rate figure of merit. Although not exact, this reference standard and the models therein have become accepted tools used in the reliability field. Part failure–rate models for a variety of components are included. These base failure rates are usually modified by π factors to improve the model accuracy.

Accelerated life test data provides the most accurate measure of a part's reliability. Since life testing can be time consuming and expensive, only the most critical parts (or an entire assembly) are usually tested. The results of life test data can be used to extrapolate the median life-time at any operating temperature (see Appendix A).

As mentioned earlier, $MTTF_{ave}$ is commonly assumed to equal $t_{50}\exp(\sigma^2/2)$, and λ_{ave} is set equal to $1/MTTF_{ave}$. This method of determining failure rate is much more accurate than the model approach of MIL–HDBK–217F, and should be used where possible. If data is not available on the exact device being used, it is often possible to obtain data on parts of similar technology. Where justified, this usually yields improved prediction results.

3.0 Environmental and Physical Assumptions

3.1 Environmental Assumptions:

Since the reliability of a semiconductor device is very dependent on the temperature of the active area, any failure rate prediction must be based on an assumed or known maximum temperature of the base-plate that the device is attached to. For this work, the maximum temperature the base-plate will be exposed to during normal operation is assumed to be +70°C. This temperature is the worst-case for reliability concerns and is used as the "heat-sink" temperature in this investigation for determining the heat rise to the active area of the semiconductor device.

Packaging of these high power semiconductors is a major area of development. The need for efficient thermal management of the system is of primary concern. This report assumes that the device is mounted to a "carrier" fabricated from a thermally efficient material sufficient to conduct heat through the interfaces of the system and maintain the assumed "heat-sink" temperature at the surface where the device (die) is attached.

3.2 Physical Assumptions:

For this work, the geometry of a unit-cell gate finger of the GaN transistor (HEMT) is assumed to be the same for every device used in the SSPA architecture. The HEMT is a generic structure typical of devices being fabricated for evaluation and benchmarking of GaN technology [3]. The unit-cell gate finger dimensions are Wg=100 μm (gate width) by Lg=0.15 μm (gate length). The gate finger is centered in a source-drain gap of 2 μm. The number of cells (gate fingers) in a given device is based on the output power required for that device.

In addition to the geometry of the active area of the device described above, this work also assumes that the generic device is fabricated on a 100 μm (4 mil) thick 4H-SiC substrate. It has been shown that an eight-finger GaN HEMT device of this cross-section has an approximate thermal resistance for the gate finger strip of 75°C/Watt [4].

The required number of unit-cell gate fingers is dependent on the power density achieved in the material and the total output power required of the device. It has been demonstrated that GaN HEMT devices of the cross-section type described above can achieve a power density of greater than 6 watts per mm at 30 GHz. For the calculations in this work, the power density of the GaN HEMT is assumed to be 6 W/mm.

Finally, gain at 1-dB compression (G @ P1dB), power-added efficiency (PAE), and output power back-off to meet linearity requirements were estimated for each device based on its location in the system block diagram. For this work, the output transistor of the high power amplifier stage was assumed to be operating at P1dB. The transistor before the output transistor was estimated to be at 4-dB back-off from P1dB, and all stages before this are at 9-dB or greater back-off from P1dB. Gain at P1dB and PAE were estimated based on total size of the device. Large devices with many fingers were assumed to have lower gain at P1dB and slightly higher PAE.

4.0 Calculation Procedures

The first step in the process of determining the reliability performance of a "system" is to calculate its expected lifetime and make sure it meets or exceeds the required MTTF. The failure-rates expected for each of the components and/or subsystems that make up the system are calculated based on their design (circuit diagrams), reliability data on the individual components used in the subsystem, and other pertinent information related to the manufacturing process. The reliability of the entire system is then calculated by summing up the failure-rates of the individual subsystems and establishing a system MTTF.

If the reliability prediction satisfies or exceeds the requirements for the system within some margin of confidence, the design is accepted based on the estimate obtained. If the reliability prediction is not satisfactory, the following options are available:

1) Review and change the manufacturing processes to more mature processes

2) Change key components to achieve a lower failure rate for that component and/or change the way their interconnection has been implemented in the given design

3) Check and change the failure rates allocated to individual components to known field-failure rates or other available data, such as actual life test data. This reduces the effect of "quality factors" used in the calculation process which may be contributing to an overly pessimistic reliability for a key component.

If the above attempts fail to produce an acceptable reliability prediction, more drastic changes in the design or technology need to be considered.

MIL–HDBK–217F provides a model specifically targeted to hybrid microcircuits. This model takes into account the fact that additional screening is performed at the hybrid assembly level. Rather than derating each failure rate at the component level for factors such as environment and quality level, the model adjusts a composite failure rate at the complete assembly level. Ideally, this yields a more accurate and less pessimistic failure rate model for complex hybrid assemblies.

Three methods are available for determining a component's base failure rate: 1) calculation based on MIL–HDBK–217F. This usually yields extremely pessimistic values; 2) predictions based on accelerated life test data. This yields the most reliable values but is often expensive, especially for microwave parts; and 3) obtain information from the supplier based on field-failure data. If field-failure data is unavailable for the specific part to be used, data on related devices or technologies may be an acceptable substitute. In such cases, the confidence level of the prediction may be less than perfect, but this still usually yields less pessimistic and more realistic values than using MIL–HDBK–217F.

5.0 Hybrid Failure Rate Calculation Method

MIL–HDBK–217F (section 5.5) defines a method for determining the reliability of a hybrid microcircuit, based on the summation of its constituent components and the application of correction (π) factors. The basic equation for hybrid reliability is presented in Equation 1.

$$\lambda_{hybrid} = \left(\sum N_C \lambda_C\right)\left(1 + 0.2\pi_E\right)\pi_F\,\pi_Q\,\pi_L \qquad \text{Eq. 1}$$

where: λ_{HYBRID} = hybrid failure rate
$\sum N_C \lambda_C$ = summation of individual component failure rates
π_E = environmental factor
π_F = circuit function factor
π_Q = quality factor
π_L = learning factor

The environmental factor (π_E) includes the effects on reliability of the environment in which it is operated. For example, the probability of a circuit failing in a cannon launch environment is much greater than the benign environment of space flight.

The circuit-function factor (π_F) is included to account for the additional stress placed on components based on their application. For instance, a device being operated in a high power dissipation application is more likely to fail than one operated with a low power dissipation. There is some debate over the values assigned in the MIL–HDBK–217F document for the categories defined. The consensus from several organizations that have reviewed the data from which the numbers were generated have suggested that the 217 values are much too conservative. The rule of thumb is to first calculate the reliability using the 217 values. If the reliability predictions are acceptable using the 217 numbers, then no further work is required. However, if additional margin is required, an acceptable refinement is to use modified numbers. Some organizations publish (π_F) factors determined from empirical data or in some cases this factor can be omitted in the analysis particularly if accelerated life test data or actual field-failure data is used.

Standard screening techniques, such as performed with class–B or –S level parts, presumably guarantee a higher level of reliability. Although there is much debate over the reality of this argument, considering the additional stress the screening methods place on the parts, MIL–HDBK–217F provides a quality factor (π_Q) adjustment which accounts for the presumed level of quality.

The learning factor (π_L) relates to the fact that as a process matures it becomes more reliable. As assembly and test techniques are refined, less tuning and/or rework is required. Hence, product quality is enhanced. This factor is based on years of experience with the technology being used, not the specific product under consideration. For instance, an assembly/test facility may have been manufacturing microwave hybrid circuits for ten years. Even though the product being analyzed has only been in production for one year, the π_L factor would be set to 10.

Per the rationale of MIL–HDBK–217F, the summation of every individual component failure rate is not required. For instance, it maintains that the reliability of some passive elements, such as resistors and inductors, are so low that they need not be included in the calculations (unless of course the circuit is made up primarily of these elements).

Each component has its own set of formulas for determining failure rates. In some cases, additional π–factors are included. In other cases, the models include factors with no specified default for hybrid calculations. In these cases, use the appropriate factors for the device under consideration.

Several overall observations of the MIL–HDBK–217F should be noted. First, the previous version (217E) included a model for bond wires. Since bond wires represent a real reliability concern, particularly bi–metal bonds, this should not be ignored. Hence, the 217E model for bond wires should be included in a component rollup. As with all interconnections, the bond wire count is simply the number of unique connections (i.e. multiple bond wires between common points are counted as one connection).

Another apparent discrepancy in 217F is the lack of a package reliability model. There is a package model for microcircuits, such as would house a digital IC, but it is not included in the hybrid model. For completeness, a hybrid package model should be a separate component whose reliability is included in the summation.

6.0 GaN SSPA Failure Rate Calculations

This section provides a summary of the failure-rate calculations of the various GaN SSPA architectures under consideration. The three architectures are: 1) septum binary combiner, 2) waveguide radial combiner, and 3) parallel-plate combiner. A detailed block-diagram for each architecture is shown in figures 1 through 3. Estimated gains and power levels are also shown for each stage in the block diagram.

These architectures are viable candidates for Ka-Band SSPA designs due to the low-loss combining techniques used in the implementation of the output stage. In addition, these designs also offer manufacturing advantages since the output combiner is implemented in a “waveguide-type” structure thus eliminating any substrate alignment and “tuning” requirements associated with planar transmission-line combiners.

Figure 1: Septum Binary Combiner SSPA Architecture Block Diagram

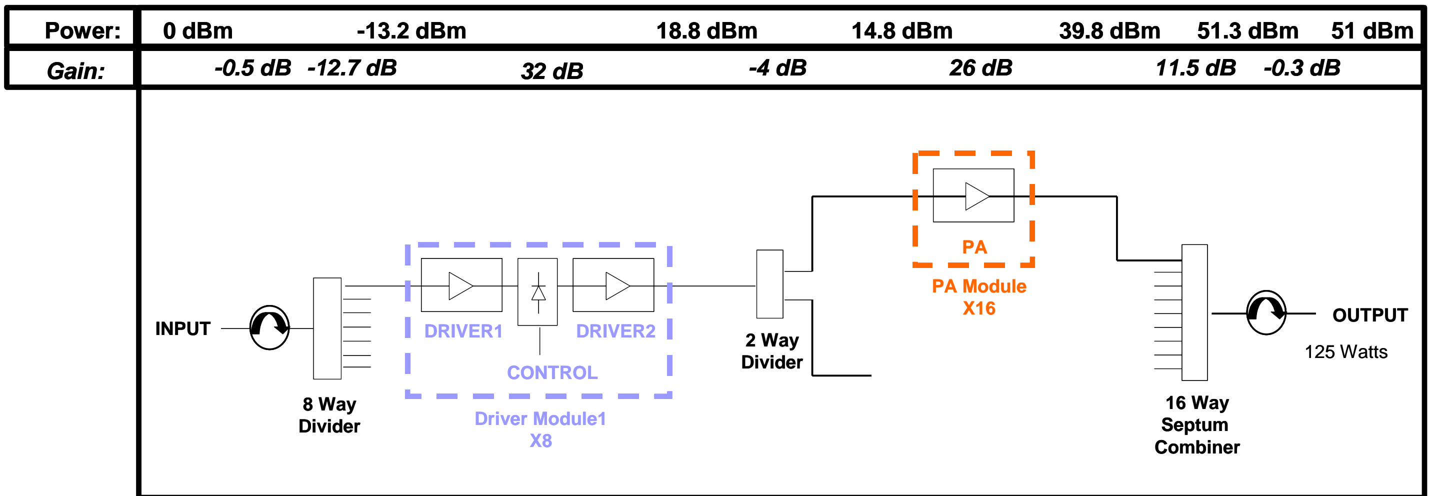


Figure 2: Waveguide Radial Combiner SSPA Architecture Block Diagram

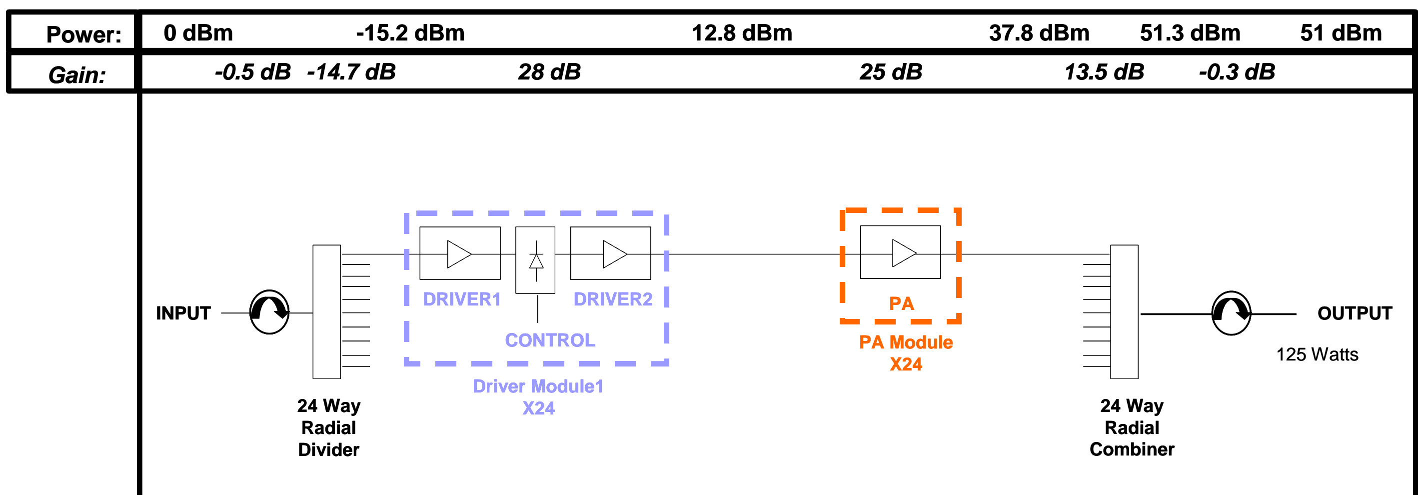
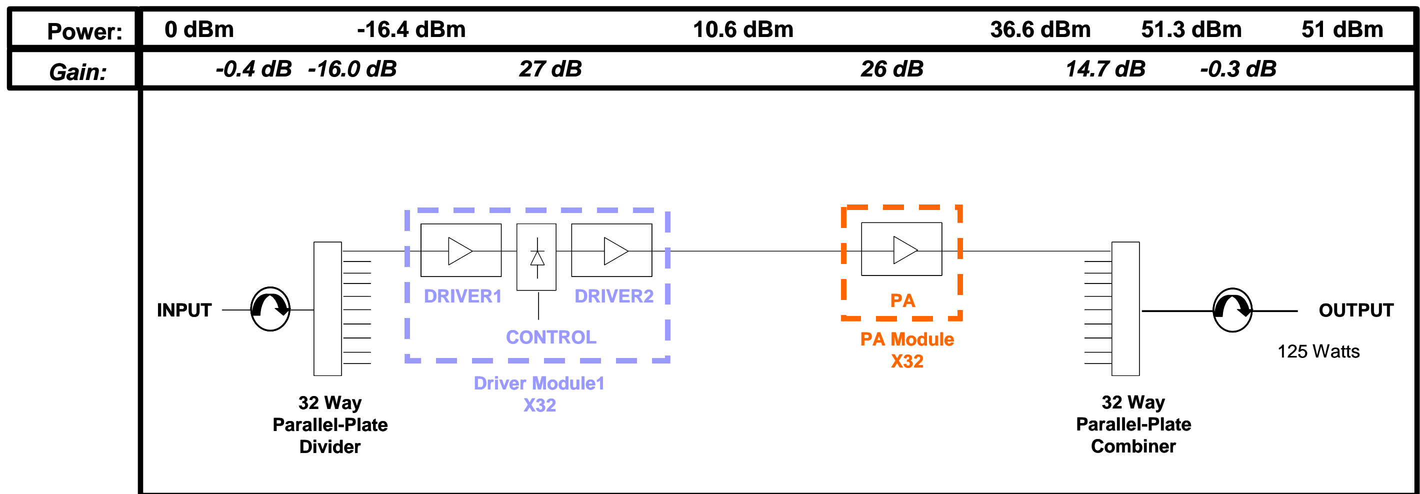


Figure 3: Parallel-Plate Combiner SSPA Architecture Block Diagram



6.1 Simplified Calculation Method

As stated previously, the absolute MTTFs and calculated failure-rates are not of major concern at this time due to the fact that no production GaN device exists that can achieve the performance levels required. Hence, no data exists for the validity of the electrical performance or lifetime of the devices to be used. However, by applying projected "conservative" performance levels for GaN technology throughout the analysis, the relative failure-rate predictions can be rationalized for the different architectures. This can be of value in demonstrating the reliability-assurance tradeoff between the designs. Therefore, to make the failure-rate calculation simple the following is noted:

1) all π-factors are given the value of 1.

2) PAE goals are used to calculate the input DC power (Pin_{dc}) required. The DC power is used to calculate the total power dissipated (Pdiss) at two operating levels, P1dB and "no-RF" drive. Based on (Pin_{dc}) and (Pdiss), the average device channel temperature (Tch_{AVG}) is calculated for "P1dB" and "no-RF" drive conditions.

3) Failure Rate Results – The failure rates assume that the amplifiers are designed as "Class A" operation. For simplicity all failure-rates are given for the "no-RF" drive condition (i.e. maximum Pdiss). This allows the analysis to disregard the issue of operational duty-cycle of RF to no-RF (i.e. least Pdiss to maximum Pdiss) correspondingly duty-cycling the channel temperature (i.e. the failure-rate) of the devices. Therefore, for failure-rate calculations the Tch_{AVG} is at "no RF" drive and assumes a constant heat-sink temperature of +70°C. This simplified analysis will produce an unrealistic and very pessimistic failure-rate.

4) Tch_{AVG} is assumed to be constant across the periphery of the device. This will usually yield a more optimistic failure-rate since the temperature gradient in the device will have "hot-spots" due to thermal coupling between adjacent cells. For

further information on the thermal profile across the device see reference [4]. In reality it is expected that the temperature will vary from finger to finger by +/-5 degrees.

5) Thermal resistance for multi-gate structures must be modified to account for intersection of the thermal fluxes between adjacent cells. For this work, the methodology of reference [4] is assumed. All devices used are the same generic gate unit-cell physical size (see paragraph 3.2).

6) The anticipated median-life versus temperature (i.e. activation energy) of GaN HEMT device technology is shown in figure 4.

7) MTTF is equal to median-life and Failure-Rate (λ) is equal to 1/MTTF.

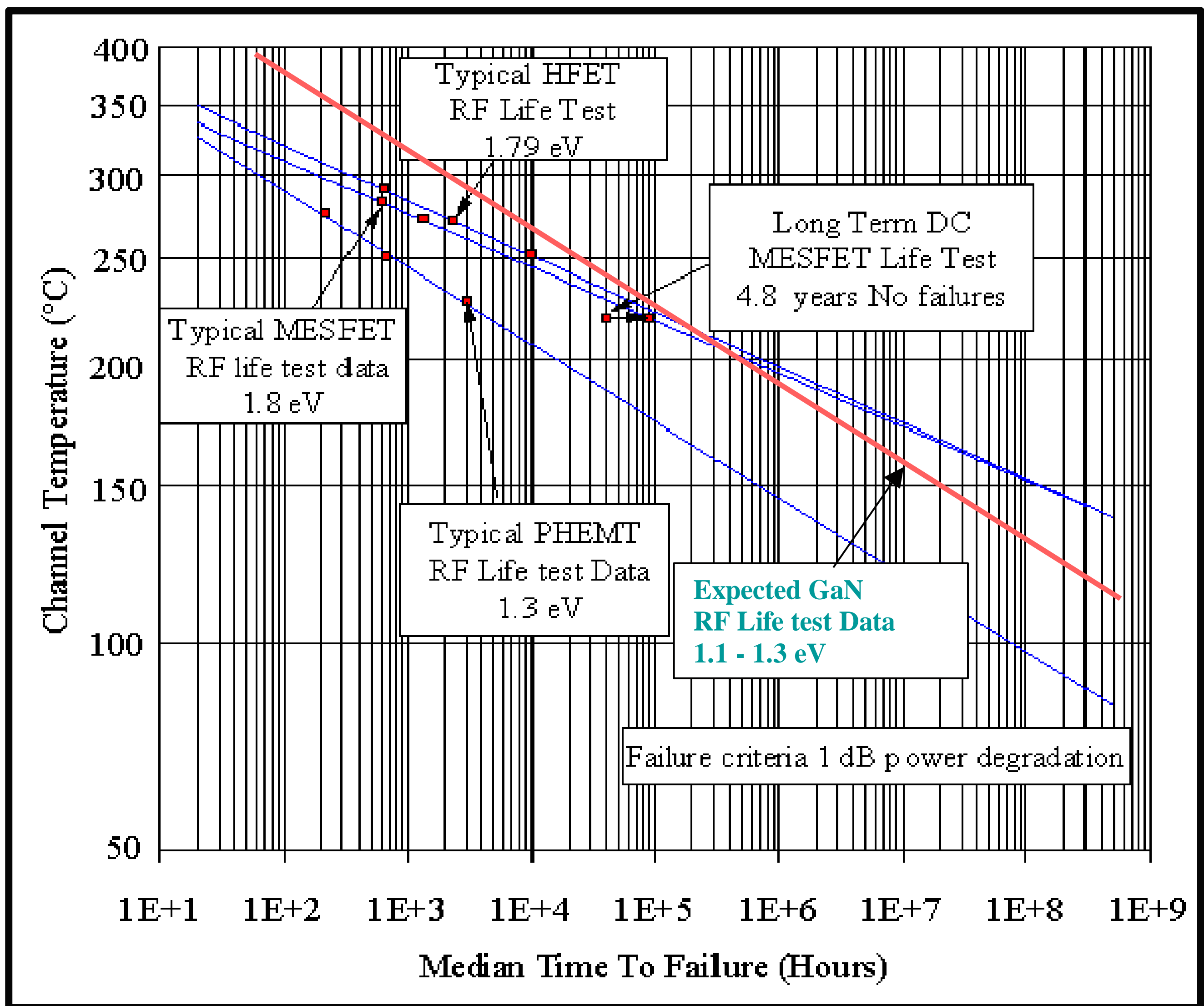


Figure 4: Anticipated GaN HEMT Technology Median-Life versus Temperature Plot

6.2 Rational for expected GaN HEMT device parameters:

Expected GaN HEMT device parameters are extrapolated from the following rational:

1) Power density is based on measured power density of single-cell devices and is stated as 6 watts/mm. This represents state-of-the art as of 2003 [2].

2) Gain at P1dB is derived from measured gain at P1dB for a single-cell device adjusted for combining several fingers to achieve the required Pout. For instance, single finger HEMT devices have demonstrated 10 to 12 dB linear gain [8], therefore, gain at P1dB would be approximately 9-11 dB. A two finger device is then assumed to achieve 9dB gain at P1dB, a 5 finger device is then 8.5 dB gain at P1dB, and a 10 finger device is 8.0 dB gain at P1 dB. The combining loss comes from the effect of amplitude and phase errors associated with the physical path-length variances of the multiple fingers.

3) Proposed GaN MMIC devices are derived from currently available GaAs PHEMT MMIC devices. For example, three-stage GaAs PHEMT MMIC devices are available at Ka-Band frequencies that achieve 20 to 30 dB of gain. Therefore, it is assumed that GaN MMIC devices will be capable of similar gain performance with correspondingly the same number of stages. Additionally, 2-watt GaAs PHEMT MMIC devices are available today. Given that GaN power density is ~4.5 times the power density of GaAs, a power output of ~9 watts is feasible in GaN technology.

6.3 Septum Binary Combiner SSPA Failure-Rate Calculation

From the block diagram of figure 1, the Septum Binary Combiner requires sixteen power amplifier modules (PA) and eight variable gain amplifier (VGA) driver modules. Based on the mechanical configuration of the septum combiner architecture, most likely the input 8-way divider and secondary 2-way divider will be implemented as microstrip Wilkinson topologies on a common microwave laminate or ceramic substrate. The output combiner will be a low-loss waveguide septum binary type circuit. The failure-rate calculation will focus only on the contribution of the PA modules and the VGA driver modules.

6.3.1 <u>Power Amplifier (PA) module MMIC Design</u>

The PA module requires an output power of approximately 9 watts (39.8 dBm) with a gain of 26 dB. Based on current GaAs PHEMT MMIC technology, the PA module will be realized as a three stage GaN MMIC.

6.3.1.1 Output Stage Transistor

Working from the output back to the input will develop the design of the individual stages of the MMIC. Since the MMIC must output 9.1 watts of power and the power density of GaN is 6 watts/mm, the periphery of the output stage must be ~1.5mm (9.1/6.0=1.5). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~9 watts of output power is 15 (1.5 / 0.1=15).

Assuming that a 15-finger device will achieve ~7.8 dB of gain at P1dB, the input power to this stage is required to be 32 dBm or 1.6 watts. Therefore, the RF power added is 9.1-1.6 watts or

7.3 watts. Assuming a power-added efficiency (PAE) for this GaN transistor of 49% at P1dB, the input power (DC) can be calculated to be 15.3 watts (Pdc=7.3/.49).

The power dissipated (Pdiss) in this transistor with “no RF” is the DC power of 15.3 watts and Pdiss at P1dB RF drive condition is 7.8 watts (15.3-7.3). Assuming that the power is evenly distributed across the 15 fingers, the power dissipated per finger is ~1 watt at “no RF” and 0.52 watts at P1dB conditions, respectively.

Finally, assuming that the thermal resistance for a 15 finger device is 84°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 84°C and 43°C for the “no RF” and P1dB conditions, respectively.

6.3.1.2 Second Stage Transistor

Since the output stage is operating at a non-linear condition (P1dB), it is desirable to have all other stages operating at an output power that is backed-off from the P1dB point. For this analysis the transistor before the output transistor is to be at 4-dB back-off from P1dB, and all stages before this are at 9-dB or greater back-off from P1dB. As shown above, the second stage must output 1.6 watts (32 dBm) of power to drive the last stage transistor. Therefore, this transistor must have 36 dBm (4 watts) of output power at P1dB in order to achieve 32 dBm at 4 dB back-off level.

Again assuming a power density of 6 watts/mm, a 4 watt output power capability requires 0.7mm of gate periphery (4/6=0.7mm). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~4 watts of output power is 7 (0.7 /0.1=7).

Assuming that a 7-finger device will achieve ~8.5 dB of gain at P1dB, the input power to this stage for P1dB is required to be 27.5 dBm or ~0.6 watts. Therefore, the RF power added is 4.0-0.6 watts or 3.4 watts. Assuming a power-added efficiency (PAE) for this GaN transistor of 49% at P1dB, the input power (DC) can be calculated to be ~6.8 watts (Pdc=3.4/.49).

Since this stage is operated at 4-dB backoff or 1.6 watts with a gain of ~9.5 dB, the PAE will be reduced. The input power to achieve the 1.6 watts (32 dBm) output is 0.180 watts (22.5 dBm). Therefore, the RF power added is 1.6-0.18 watts or 1.42 watts. The PAE at this operating point is only 21%. The power dissipated (Pdiss) in this transistor with “no RF” is the DC power of 6.8 watts and the Pdiss at 1.6 watts RF drive condition is ~5.4 watts (6.8-1.42). Assuming that the power is evenly distributed across the 7 fingers, the power dissipated per finger is ~0.96 watts at “no RF” and 0.77 watts at 4 dB back-off conditions, respectively.

Finally, assuming that the thermal resistance for a seven finger device is 75°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 72°C and 58°C for the “no RF” and 4 dB back-off conditions, respectively.

6.3.1.3 First Stage Transistor

As shown above, the first stage must output 0.18 watts (22.5 dBm) of power to drive the second stage transistor. Therefore, this transistor must have 31~ dBm (1.25 watts) of output power at P1dB in order to achieve 22 dBm at 9 dB back-off level.

Again assuming a power density of 6 watts/mm, 1.25 watts of output power capability requires 0.2mm of gate periphery (1.25/6=0.2mm). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~1.2 watts of output power is 2 (0.2 /0.1=2).

Assuming that a 2-finger device will achieve ~9.0 dB of gain at P1dB, the input power to this stage for P1dB is required to be 22.5 dBm or ~0.18 watts. Therefore, the RF power added is 1.25-0.18 watts or 1 watt. Assuming a power-added efficiency (PAE) for this GaN transistor of 49% at P1dB, the input power (DC) can be calculated to be ~2 watts (Pdc=1/.49).

Since this stage is operated at 9-dB backoff or 0.18 watts with a gain of ~10 dB, the PAE will be reduced. The input power to achieve the 0.18 watts (22.5 dBm) output is 0.018 watts (12.5 dBm). Therefore, the RF power added is 0.18-0.018 watts or 0.162 watts. The PAE at this operating point is only 9%. The power dissipated (Pdiss) in this transistor with “no RF” is the DC power of 2 watts and the Pdiss at 0.18 watts RF drive condition is ~1.8 watts (2.0-.18). Assuming that the power is evenly distributed across the 2 fingers, the power dissipated per finger is ~1 watts at “no RF” and 0.9 watts at 9 dB back-off conditions, respectively.

Finally, assuming that the thermal resistance for a two-finger device is 63.6^{O}C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 63.6^{O}C and 57°C for the “no RF” and 9 dB back-off conditions, respectively.

6.3.1.4 Power Amplifier (PA) module MMIC Failure-Rate Calculation

The PA module is implemented with a three-stage GaN MMIC as shown in figure 5. The failure-rate is a function of the channel temperature of the active devices. For this analysis, the heat-sink temperature is assumed as a constant of 70ºC and the power dissipation in each transistor is calculated at the worst-case condition of “no-RF” drive. MTTF is determined from figure 4.

Power:	**12.5 dBm**		**22.5 dBm**		**32.0 dBm**		**39.8 dBm**
Gain:		***10.0 dB***		***9.5 dB***		***7.8 dB***	
MTTF:		**1.3 x 10^8 hrs.**		**2.5 x 10^7 hrs.**		**1.35 x 10^7 hrs.**	
Fr:		***0.008 kfits***		***0.04 kfits***		***0.074 kfits***	

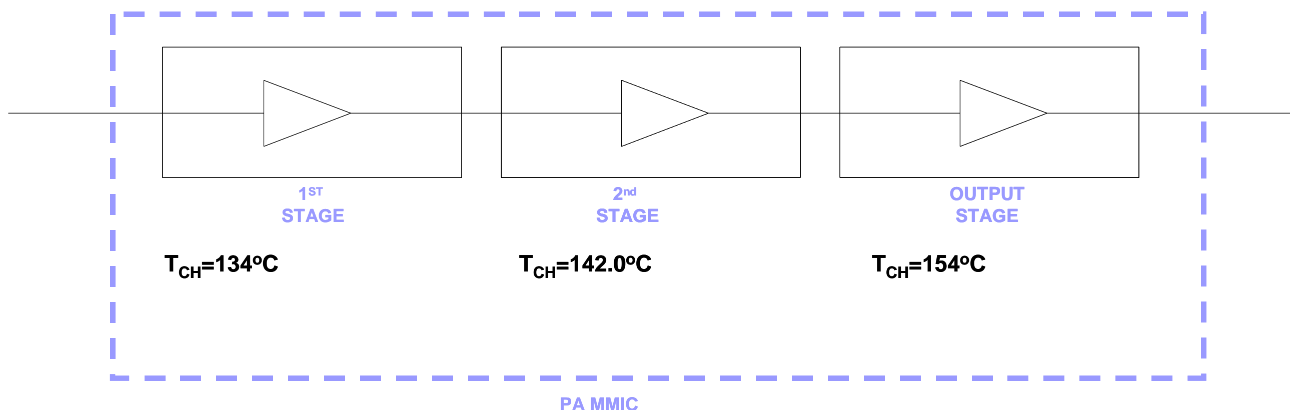


Figure 5: Three-Stage 9.1-Watt GaN MMIC Device

6.3.2 Variable Gain Amplifier (VGA) module MMIC Design

The VGA module requires an output power of approximately .08 watts (19 dBm) with a gain of 32 dB. The gain must be adjustable by ~10 dB in order to account for variations in path loss and PA MMIC gain mismatch. The VGA will consist of a three-stage input MMIC, a single-stage variable attenuator MMIC, and a two-stage output MMIC.

6.3.2.1 Output two-stage MMIC

As stated above, this MMIC must output 0.08 watts (19 dBm) of power to drive the PA module. Therefore, this transistor must have ~29 dBm (0.8 watts) of output power at P1dB in order to achieve 19 dBm at 10 dB back-off level.

This transistor is equivalent to the two-finger input stage of the PA module. However, the bias input can be reduced on this device since the P1dB point is 2-3 dB less. Assuming the DC power is 1.8 watts and evenly distributed across the 2 fingers, the power dissipated per finger is ~.9 watts at "no RF" and 0.8 watts at 10 dB back-off conditions, respectively.

Assuming that the thermal resistance for a two-finger device is 63.6^{O}C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 57°C and 51°C for the "no RF" and 10 dB back-off conditions, respectively.

The input transistor can be the same two-finger device with reduced bias conditions of ~1.2 watts at "no-RF". Assuming that the thermal resistance for a two-finger device is 63.6^{O}C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 38°C.

6.3.2.2 Variable Attenuator MMIC

The variable attenuator MMIC will most likely be a FET based attenuator with gain versus gate bias control. Very little power dissipation is expected from this stage, therefore, the failure rate will be assumed to be equal to a transistor channel of 32°C rise above the heat-sink.

6.3.2.3 Input Three-Stage MMIC

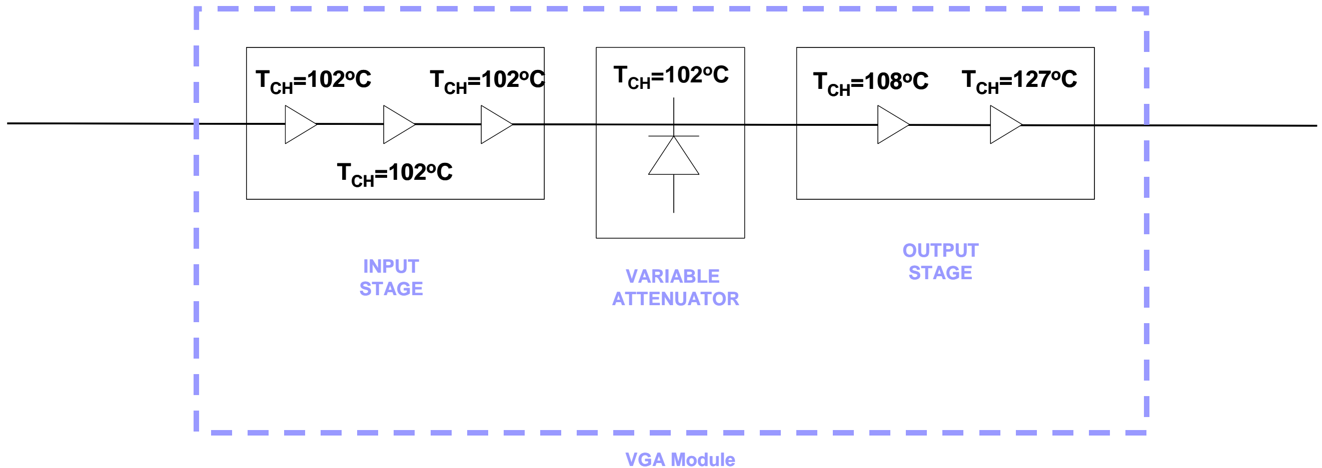
All three transistor can be a two-finger device with reduced bias conditions of ~1.0 watt at "no-RF". Assuming that the thermal resistance for a two-finger device is 63.6^{O}C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 32°C.

6.3.2.4 Variable Gain Amplifier (VGA) module MMIC Failure-Rate Calculation

The VGA module is implemented as shown in figure 6. The failure-rate is a function of the channel temperature of the active devices. For this analysis, the heat-sink temperature is assumed as a constant of 70ºC and the power dissipation in each transistor is calculated at the worst-case condition of "no-RF" drive. The MTTF is determined from figure 4.

Figure 6: 0.8 watt (+29dBm) GaN VGA MMIC Module

Power:	**-13.2 dBm**		**11.8 dBm**		**3.8 dBm**		**18.8 dBm**
Gain:		***25.0 dB***		***-8.0 dB***		***15.0 dB***	
MTTF:		**6.6 x 10^8 hrs.**		**2.0 x 10^9 hrs.**		**1.7 x 10^8 hrs.**	
Fr:		***0.0015 kfits***		***0.0005 kfits***		***0.006 kfits***	



6.4 Waveguide Radial Combiner SSPA Failure-Rate Calculation

From the block diagram of figure 2, the Waveguide Radial Combiner requires twenty-four power amplifier modules (PA) and twenty-four variable gain amplifier (VGA) driver modules. Based on the mechanical configuration, the input divider and output combiner will be implemented as a low-loss waveguide radial topology. The failure-rate calculation will focus only on the contribution of the PA modules and the VGA driver modules.

6.4.1 Power Amplifier (PA) module MMIC Design

The PA module requires an output power of approximately 6.0 watts (37.8 dBm) with a gain of 25 dB. Based on current GaAs PHEMT MMIC technology, the PA module will be realized as a three stage GaN MMIC.

6.4.1.1 Output Stage Transistor

Working from the output back to the input will develop the design of the individual stages of the MMIC. Since the MMIC must output 6.0 watts of power and the power density of GaN is 6 watts/mm, the periphery of the output stage must be ~1.0mm (6.0/6.0=1.0). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~6 watts of output power is 10 (1.0 / 0.1=10).

Assuming that a 10-finger device will achieve ~8.0 dB of gain at P1dB, the input power to this stage is required to be 30 dBm or 1.0 watts. Therefore, the RF power added is 6.0-1.0 watts or 5.0 watts. Assuming a power-added efficiency (PAE) for this GaN transistor of 48% at P1dB, the input power (DC) can be calculated to be 10.4 watts (Pdc=5.0/.48).

The power dissipated (Pdiss) in this transistor with "no RF" is the DC power of 10.4 watts and Pdiss at P1dB RF drive condition is 5.4 watts (10.4-5.0). Assuming that the power is evenly distributed across the 10 fingers, the power dissipated per finger is ~1 watt at "no RF" and 0.54 watts at P1dB conditions, respectively.

Finally, assuming that the thermal resistance for a 10 finger device is 77°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 77°C and 42°C for the "no RF" and P1dB conditions, respectively.

6.4.1.2 Second Stage Transistor

Since the output stage is operating at a non-linear condition (P1dB), it is desirable to have all other stages operating at an output power that is backed-off from the P1dB point. For this analysis the transistor before the output transistor is to be at 4-dB back-off from P1dB, and all stages before this are at 9-dB or greater back-off from P1dB. As shown above, the second stage must output 1.0 watts (30 dBm) of power to drive the last stage transistor. Therefore, this transistor must have 34 dBm (2.5 watts) of output power at P1dB in order to achieve 30 dBm at 4 dB back-off level.

Again assuming a power density of 6 watts/mm, a 2.5 watt output power capability requires 0.42mm of gate periphery (2.5/6=0.42mm). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~2.5 watts of output power is 5 (0.42 /0.1=4.2).

Assuming that a 5-finger device will achieve ~8.5 dB of gain at P1dB, the input power to this stage for P1dB is required to be 25.5 dBm or ~0.35 watts. Therefore, the RF power added is 2.5-0.35 watts or 2.15 watts. Assuming a power-added efficiency (PAE) for this GaN transistor of 48% at P1dB, the input power (DC) can be calculated to be ~4.5 watts (Pdc=2.15/.48).

Since this stage is operated at 4-dB backoff or 1.0 watts with a gain of ~9.5 dB, the PAE will be reduced. The input power to achieve the 1.0 watts (30 dBm) output is 0.12 watts (20.5 dBm). Therefore, the RF power added is 1.0-0.12 watts or 0.88 watts. The PAE at this operating point is only 20%. The power dissipated (Pdiss) in this transistor with "no RF" is the DC power of 4.5 watts and the Pdiss at 1.0 watts RF drive condition is ~3.62 watts (4.5-.88). Assuming that the power is evenly distributed across the 5 fingers, the power dissipated per finger is ~0.9 watts at "no RF" and 0.72 watts at 4 dB back-off conditions, respectively.

Finally, assuming that the thermal resistance for a 5 finger device is 71°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 64°C and 51°C for the "no RF" and 4 dB back-off conditions, respectively.

6.4.1.3 First Stage Transistor

As shown above, the first stage must output 0.12 watts (20.5 dBm) of power to drive the second stage transistor. Therefore, this transistor must have 30~ dBm (1.0 watts) of output power at P1dB in order to achieve ~21 dBm at 9 dB back-off level.

Again assuming a power density of 6 watts/mm, 1.0 watts of output power capability requires 0.2mm of gate periphery (1.0/6=0.17mm). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~1.0 watts of output power is 2 (0.17 /0.1=1.7).

Assuming that a 2-finger device will achieve ~9.0 dB of gain at P1dB, the input power to this stage for P1dB is required to be 21.0 dBm or ~0.125 watts. Therefore, the RF power added is 1.0-0.125 watts or 0.88 watts. Assuming a power-added efficiency (PAE) for this GaN transistor of 48% at P1dB, the input power (DC) can be calculated to be ~1.8 watts (Pdc=.88/.48).

Since this stage is operated at 9-dB backoff or 0.12 watts with a gain of ~10 dB, the PAE will be reduced. The input power to achieve the 0.12 watts (20.5 dBm) output is 0.012 watts (10.5 dBm). Therefore, the RF power added is 0.12-0.012 watts or 0.108 watts. The PAE at this operating point is only 6%. The power dissipated (Pdiss) in this transistor with "no RF" is the DC power of 1.8 watts and the Pdiss at 0.12 watts RF drive condition is ~1.7 watts (1.8-.108). Assuming that the power is evenly distributed across the 2 fingers, the power dissipated per finger is ~0.9 watts at "no RF" and 0.85 watts at 9 dB back-off conditions, respectively.

Finally, assuming that the thermal resistance for a two-finger device is 63.6°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 57°C and 54°C for the "no RF" and 9 dB back-off conditions, respectively.

6.4.1.4 Power Amplifier (PA) module MMIC Failure-Rate Calculation

The PA module is implemented with a three-stage GaN MMIC as shown in figure 7. The failure-rate is a function of the channel temperature of the active devices. For this analysis, the heat-sink temperature is assumed as a constant of 70°C and the power dissipation in each transistor is calculated at the worst-case condition of "no-RF" drive. MTTF is determined from figure 4.

Power:	**10.5 dBm**		**20.5 dBm**		**29.8 dBm**		**37.8 dBm**
Gain:		***10.0 dB***		***9.5 dB***		***8.0 dB***	
MTTF:		**1.8×10^8 hrs.**		**1.3×10^8 hrs.**		**2.2×10^7 hrs.**	
Fr:		***0.005 kfits***		***0.008 kfits***		***0.045 kfits***	

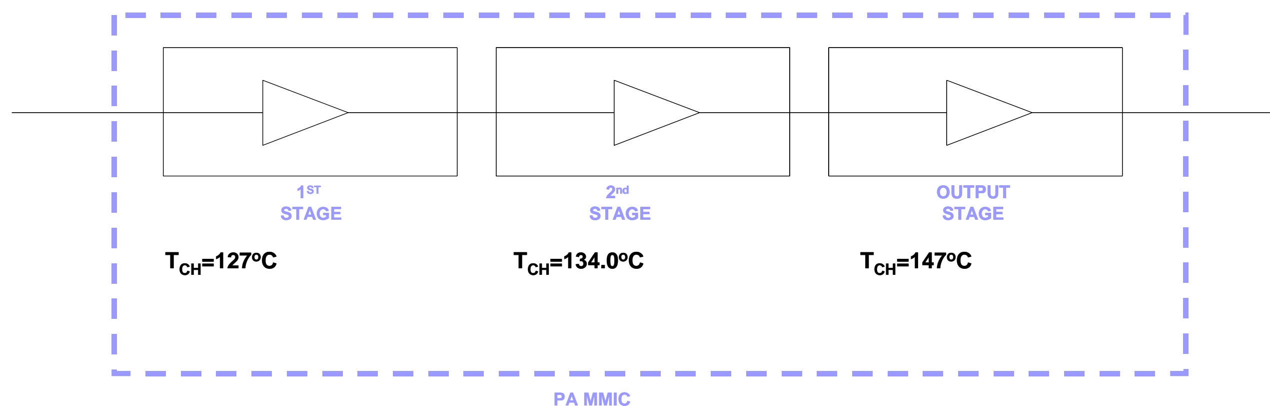


Figure 7: Three-Stage 6.0-Watt GaN MMIC Device

6.4.2 Variable Gain Amplifier (VGA) module MMIC Design

The VGA module requires an output power of approximately .02 watts (13 dBm) with a gain of 28 dB. The gain must be adjustable by ~10 dB in order to account for variations in path loss and PA MMIC gain mismatch. The VGA will consist of a three-stage input MMIC, a single-stage variable attenuator MMIC, and a two-stage output MMIC.

6.4.2.1 Output two-stage MMIC

As stated above, this MMIC must output 0.02 watts (13 dBm) of power to drive the PA module. Therefore, this transistor must have ~23 dBm (0.2 watts) of output power at P1dB in order to achieve 13 dBm at 10 dB back-off level.

This transistor is equivalent to the two-finger input stage of the PA module. However, the bias input can be reduced on this device since the P1dB point is 2-3 dB less. Assuming the DC power is 1.2 watts and evenly distributed across the 2 fingers, the power dissipated per finger is ~.6 watts at "no RF" and 0.55 watts at 10 dB back-off conditions, respectively.

Assuming that the thermal resistance for a two-finger device is 63.6^{O}C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 38°C and 35°C for the "no RF" and 10 dB back-off conditions, respectively.

The input transistor can be the same two-finger device with reduced bias conditions of ~1.0 watts at "no-RF". Assuming that the thermal resistance for a two-finger device is 63.6^{O}C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 32°C.

6.4.2.2 Variable Attenuator MMIC

The variable attenuator MMIC will most likely be a FET based attenuator with gain versus gate bias control. Very little power dissipation is expected from this stage, therefore, the failure rate will be assumed to be equal to a transistor channel of 32°C rise above the heat-sink.

6.4.2.3 Input Three-Stage MMIC

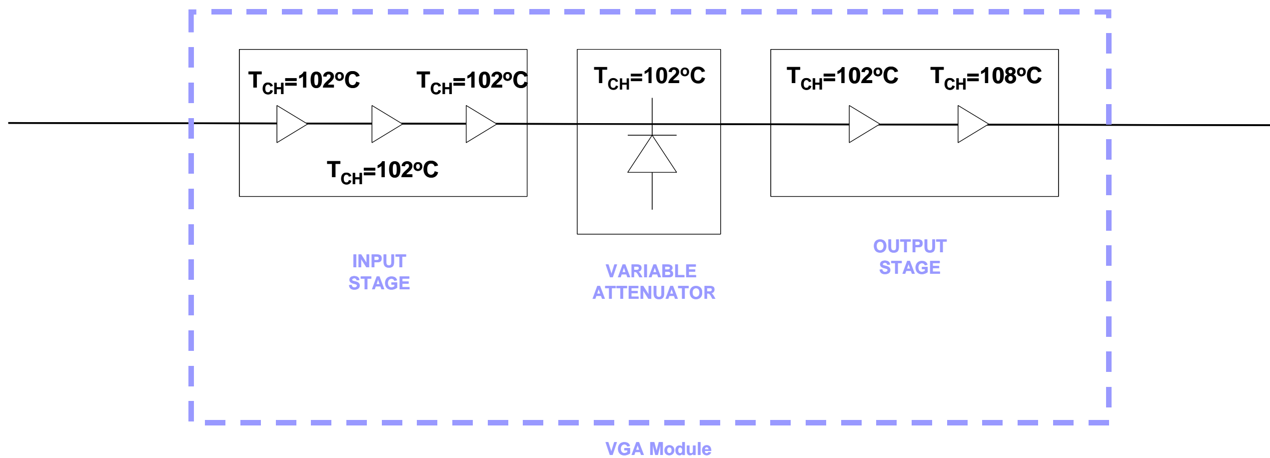
All three transistor can be a two-finger device with reduced bias conditions of ~1.0 watt at "no-RF". Assuming that the thermal resistance for a two-finger device is 63.6^{O}C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 32°C.

6.4.2.4 Variable Gain Amplifier (VGA) module MMIC Failure-Rate Calculation

The VGA module is implemented as shown in figure 8. The failure-rate is a function of the channel temperature of the active devices. For this analysis, the heat-sink temperature is assumed as a constant of 70°C and the power dissipation in each transistor is calculated at the worst-case condition of "no-RF" drive. The MTTF is determined from figure 4.

Figure 8: 0.20 Watt (+23dBm) GaN VGA MMIC Module

Power:	**-15.0 dBm**		**10.0 dBm**		**-2 dBm**		**13 dBm**
Gain:		***25.0 dB***		***-12.0 dB***		***15.0 dB***	
MTTF:		**6.6 x 10^8 hrs.**		**2.0 x 10^9 hrs.**		**6.6 x 10^8 hrs.**	
Fr:		***0.0015 kfits***		***0.0005 kfits***		***0.0015 kfits***	



6.5 Parallel-Plate Combiner SSPA Failure-Rate Calculation

From the block diagram of figure 3, the Parallel-Plate Combiner requires thirty-two power amplifier modules (PA) and thirty-two variable gain amplifier (VGA) driver modules. Based on the mechanical configuration, the input divider and output combiner will be implemented as a low-loss parallel-plate radial topology. The failure-rate calculation will focus only on the contribution of the PA modules and the VGA driver modules.

6.5.1 <u>Power Amplifier (PA) module MMIC Design</u>

The PA module requires an output power of approximately 4.5 watts (36.6 dBm) with a gain of 26 dB. Based on current GaAs PHEMT MMIC technology, the PA module will be realized as a three stage GaN MMIC.

6.5.1.1 Output Stage Transistor

Working from the output back to the input will develop the design of the individual stages of the MMIC. Since the MMIC must output 4.5 watts of power and the power density of GaN is 6 watts/mm, the periphery of the output stage must be ~0.75mm (4.5/6.0=0.75). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~4.5 watts of output power is 8 (0.75 / 0.1=7.5).

Assuming that an 8-finger device will achieve ~8.5 dB of gain at P1dB, the input power to this stage is required to be 28 dBm or 0.63 watts. Therefore, the RF power added is 4.5-0.63 watts

or 3.9 watts. Assuming a power-added efficiency (PAE) for this GaN transistor of 48% at P1dB, the input power (DC) can be calculated to be 8.0 watts (Pdc=3.9/.48).

The power dissipated (Pdiss) in this transistor with “no RF” is the DC power of 8.0 watts and Pdiss at P1dB RF drive condition is 4.1 watts (8.0-3.9). Assuming that the power is evenly distributed across the 8 fingers, the power dissipated per finger is ~1 watt at “no RF” and 0.51 watts at P1dB conditions, respectively.

Finally, assuming that the thermal resistance for an 8 finger device is 75°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 75°C and 38°C for the “no RF” and P1dB conditions, respectively.

6.5.1.2 Second Stage Transistor

Since the output stage is operating at a non-linear condition (P1dB), it is desirable to have all other stages operating at an output power that is backed-off from the P1dB point. For this analysis the transistor before the output transistor is to be at 4-dB back-off from P1dB, and all stages before this are at 9-dB or greater back-off from P1dB. As shown above, the second stage must output 0.63 watts (28 dBm) of power to drive the last stage transistor. Therefore, this transistor must have 32 dBm (1.6 watts) of output power at P1dB in order to achieve 28 dBm at 4 dB back-off level.

Again assuming a power density of 6 watts/mm, a 1.6 watt output power capability requires 0.42mm of gate periphery (1.6/6=0.26mm). Based on the standard gate finger width of 100 μm (0.1 mm), the total number of gate fingers required for ~1.6 watts of output power is 3 (0.26 /0.1=2.6).

Assuming that a 3-finger device will achieve ~8.8 dB of gain at P1dB, the input power to this stage for P1dB is required to be 23.2 dBm or ~0.21 watts. Therefore, the RF power added is 1.6-0.21 watts or 1.4 watts. Assuming a power-added efficiency (PAE) for this GaN transistor of 48% at P1dB, the input power (DC) can be calculated to be ~2.9 watts (Pdc=1.4/.48).

Since this stage is operated at 4-dB backoff or 0.63 watts with a gain of ~9.8 dB, the PAE will be reduced. The input power to achieve the 0.63 watts (28 dBm) output is 0.065 watts (18.2 dBm). Therefore, the RF power added is 0.63-0.065 watts or 0.56 watts. The PAE at this operating point is only 19%. The power dissipated (Pdiss) in this transistor with “no RF” is the DC power of 2.9 watts and the Pdiss at 0.63 watts RF drive condition is ~2.34 watts (2.9-0.56). Assuming that the power is evenly distributed across the 3 fingers, the power dissipated per finger is ~0.97 watt at “no RF” and 0.78 watts at 4 dB back-off conditions, respectively.

Finally, assuming that the thermal resistance for a 3 finger device is 65°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 64°C and 51°C for the “no RF” and 4 dB back-off conditions, respectively.

6.5.1.3 First Stage Transistor

As shown above, the first stage must output 0.065 watts (18.2 dBm) of power to drive the second stage transistor. Therefore, this transistor must have ~27 dBm (0.5 watts) of output power at P1dB in order to achieve ~18 dBm at 9 dB back-off level.

This transistor can be similar to the last stage transistor of the +29dBm VGA module of paragraph 6.3.2.1. Assuming the DC power is 1.8 watts and evenly distributed across the 2 fingers, the power dissipated per finger is ~.9 watts at "no RF" and 0.8 watts at 10 dB back-off conditions, respectively.

Assuming that the thermal resistance for a two-finger device is 63.6°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 57°C and 51°C for the "no RF" and 10 dB back-off conditions, respectively.

6.5.1.4 Power Amplifier (PA) module MMIC Failure-Rate Calculation

The PA module is implemented with a three-stage GaN MMIC as shown in figure 9. The failure-rate is a function of the channel temperature of the active devices. For this analysis, the heat-sink temperature is assumed as a constant of 70°C and the power dissipation in each transistor is calculated at the worst-case condition of "no-RF" drive. MTTF is determined from figure 4.

Power:	8.2 dBm	18.2 dBm	28.0 dBm	36.6 dBm
Gain:	*10.0 dB*	*9.8 dB*	*8.6 dB*	
MTTF:	1.8×10^8 hrs.	1.3×10^8 hrs.	2.35×10^7 hrs.	
Fr:	*0.005 kfits*	*0.008 kfits*	*0.043 kfits*	

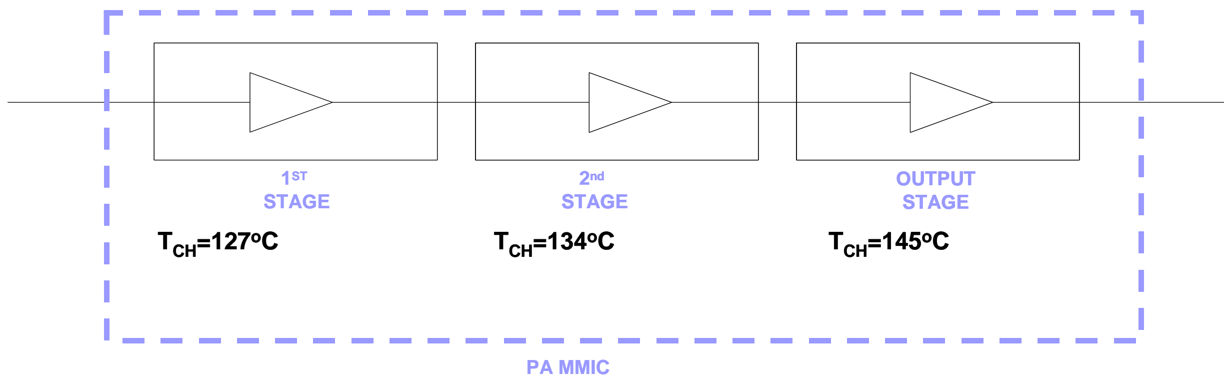


Figure 9: Three-Stage 4.5-Watt GaN MMIC Device

6.5.2 Variable Gain Amplifier (VGA) module MMIC Design

The VGA module requires an output power of approximately .012 watts (10.6 dBm) with a gain of 27 dB. The gain must be adjustable by ~10 dB in order to account for variations in path loss and PA MMIC gain mismatch. The VGA will consist of a three-stage input MMIC, a single-stage variable attenuator MMIC, and a two-stage output MMIC.

6.5.2.1 Output two-stage MMIC

As stated above, this MMIC must output 0.02 watts (13 dBm) of power to drive the PA module. Therefore, this transistor must have ~23 dBm (0.2 watts) of output power at P1dB in order to achieve 13 dBm at 10 dB back-off level.

This transistor is equivalent to the two-finger input stage of the PA module. However, the bias input can be reduced on this device since the P1dB point is 2-3 dB less. Assuming the DC power is 1.0

watts and evenly distributed across the 2 fingers, the power dissipated per finger is ~.5 watts at "no RF" and 0.45 watts at 10 dB back-off conditions, respectively.

Assuming that the thermal resistance for a two-finger device is 63.6°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 32°C and 29°C for the "no RF" and 10 dB back-off conditions, respectively.

The input transistor can be the same two-finger device with similar bias conditions of ~1.0 watts at "no-RF". Assuming that the thermal resistance for a two-finger device is 63.6°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 32°C.

6.5.2.2 Variable Attenuator MMIC

The variable attenuator MMIC will most likely be a FET based attenuator with gain versus gate bias control. Very little power dissipation is expected from this stage, therefore, the failure rate will be assumed to be equal to a transistor channel of 32°C rise above the heat-sink.

6.5.2.3 Input Three-Stage MMIC

All three transistor can be a two-finger device with reduced bias conditions of ~1.0 watt at "no-RF". Assuming that the thermal resistance for a two-finger device is 63.6°C/watt, the temperature rise of the transistor channel above the heat-sink is approximately 32°C.

6.5.2.4 Variable Gain Amplifier (VGA) module MMIC Failure-Rate Calculation

The VGA module is implemented as shown in figure 10. The failure-rate is a function of the channel temperature of the active devices. For this analysis, the heat-sink temperature is assumed as a constant of 70°C and the power dissipation in each transistor is calculated at the worst-case condition of "no-RF" drive. The MTTF is determined from figure 4.

Power:	**-19.4 dBm**	**5.6 dBm**	**-4.4 dBm**	**10.6 dBm**
Gain:	***25.0 dB***	***-10.0 dB***	***15.0 dB***	
MTTF:	**6.6 x 10^8 hrs.**	**2.0 x 10^9 hrs.**	**1.0 x 10^9 hrs.**	
Fr:	***0.0015 kfits***	***0.0005 kfits***	***0.0010 kfits***	

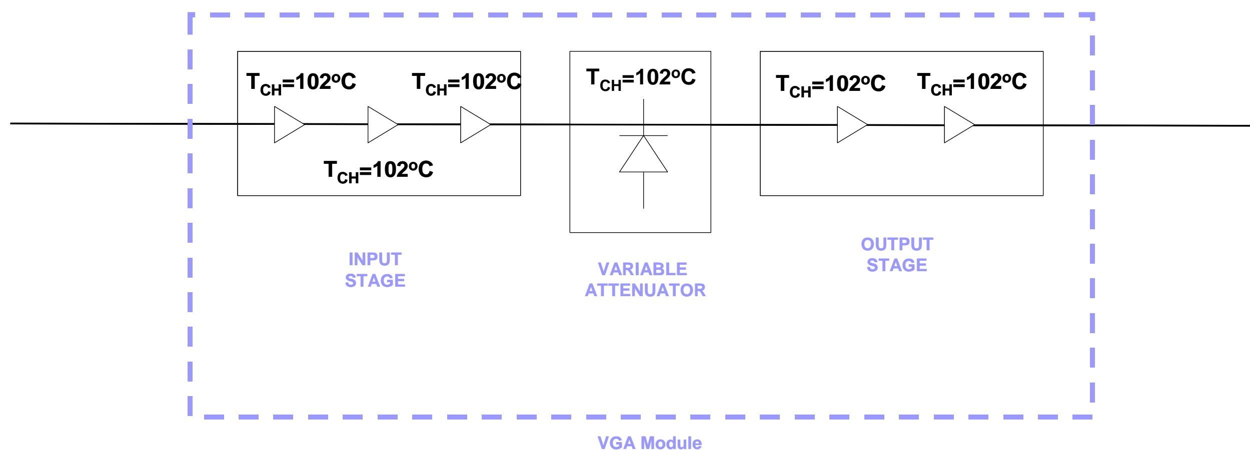


Figure 10: 0.10 Watt (+20dBm) GaN VGA MMIC Module

6.6 SSPA Reliability Summary

Table 1 presents a summary of the predicted failure rate and the related MTTF for the three SSPA architectures of interest. As stated previously, the absolute MTTFs and calculated failure-rates are not of major concern at this time due to the fact that no production GaN device exists that can achieve the performance levels required. Hence, no data exists for the validity of the electrical performance or lifetime of the devices to be used. However, by applying projected "conservative" performance levels for GaN technology throughout the analysis, the relative failure-rate predictions can be rationalized for the different architectures. This can be of value in demonstrating the reliability-assurance tradeoff between the designs.

Table 1 lists the three architectures in the ranking of most reliable to least reliable. The most reliable architecture is normalized to a value of 1.

Table 1: GaN SSPA Reliability Summary

JPL WBG SSPA Component Summary						
Architecture	Device Type	Quantity	Failure Rate (kfits)	MTTF (years)	MTTF (Normalized)	Device Technology
Radial Combiner						
	HPA	24	0.058	1.724E+07		GaN 6.0 Watt
	VGA	24	0.0035	2.857E+08		GaN 0.2 Watt
Total		***48***	***1.476***	6.775E+05	100%	
Parallel-Plate Radial Combiner						
	HPA	32	0.056	1.786E+07		GaN 4.5 Watt
	VGA	32	0.003	3.333E+08		GaN 0.1 Watt
Total		***64***	***1.888***	5.297E+05	78%	
Waveguide Binary						
	HPA	16	0.122	8.197E+06		GaN 9.1 Watt
	VGA	8	0.008	1.250E+08		GaN 0.8 Watt
Total		***24***	***2.016***	4.960E+05	73%	

[1] John C. Zolper, “STAR on Wide Bandgap RF Technology”, Working Group A Special Technology Area Review, April 2000.

[2] J. W. Johnson, et al, “Performance of AlGaN/GaN High Electron Mobility Transistors at Nanoscale Gate Lengths”, University of Florida Wide Bandgap report for Project NSF CTS9901173.

[3] Primit Parikh, et al, “GaN Power HEMTs for mm-wave Applications”, NNUN Abstracts 2002, Cree Lighting Company, Goleta, CA.

[4] Jon C. Freeman, “Channel Temperature Model for Microwave AlGaN/GaN Power HEMTs on SiC and Sapphire”, IEEE MTT-S Digest 2004.

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Appendix A: Accelerated Life Test Reliability Prediction Models

Failure rate information is useful in predicting the probability that a circuit or component will continue to function properly throughout its expected lifetime. Two methods have been adopted for determining failure rates. The first method analyzes field–return information to develop models for component groups. This is the method that was used to generate the models of MIL–HDBK–217. The second method uses measured accelerated life test results to predict failure rates. This Appendix reviews the basic concepts of reliability prediction and its association with accelerated life testing.

The failure mechanisms of electronic circuits are not constant, but vary with time. During the early life of the component, failure rates are dominated by infant mortality. Then there is a period of nearly constant failure rate, followed by an accelerated failure rate near component wear out. A plot of this effect resembles the basin of a bathtub, and hence carries the same name. Since burn–in test methods effectively weed out infant mortality failures, the constant failure–rate region is of most interest for reliability predictions.

Because the inherent lifetimes of electronic devices are measured in tens and even hundreds of years, it is often impractical to wait for a statistically significant number of normal returns to determine a part's reliability. Fortunately, failure processes in electronic devices may be accelerated by several methods, such as thermal or electrical stress. The most common failure processes (e.g. metal migration, etc.) are physio–chemical in nature and may be accelerated with temperature. The Arrhenius equation relates the rate at which a process occurs to temperature and activation energy, per Equation A–1.

$$r = A\, e^{\left[\frac{-E_a}{kT}\right]} \qquad \text{Eq. A–1}$$

where: r = rate of the process
A = a proportional multiplier, which can be a function of temperature
E_a = activation energy
K = Boltzman's constant, 8.6×10^{-5} (eV / °K)
T = temperature (°K)

By operating a device at elevated temperatures, it is possible to induce a statistically significant number of failures in an accelerated time frame. The most common failure mechanisms occur in the junctions of active devices, where the highest temperatures exist. Hence, it is critical that the junction temperature, not base temperature, be maintained constant throughout the life testing process.

The results of accelerated life testing presume a common failure mechanism. Hence, the importance of failure analysis in the life testing process. If more than one failure mechanism is present, the results must be combined in an alternate fashion.

The failure count vs. time for semiconductor devices follows a lognormal distribution, which implies the failure rate varies with and is a function of time. The instantaneous failure rate is given by Equation A-2 [1]. This equation states that the instantaneous failure rate equals the probability that a failure will occur at time t divided by the probability that no failures occurred before that time.

$$\lambda(t) = \frac{f(t)}{R(t)} = \frac{f(t)}{[1 - F(t)]} \quad \text{(fits)} \qquad \text{Eq. A–2}$$

where: $\lambda(t)$ = instantaneous failure rate
f(t) – probability density function of the lognormal distribution evaluated at time t
R(t) – reliability function, the probability that no failures have occurred before time t
F(t) – cumulative distribution function of the lognormal distribution

note: 1 fit = 1 failure in 10^9 hours

The probability density function (PDF) for the lognormal failure distribution is given by Equation A-3.

$$\text{PDF} = f(t) = \frac{1}{\sigma t \sqrt{2\pi}} \, e^{-\frac{1}{2}\left(\frac{\ln(t) - \ln(t_{50})}{\sigma}\right)^2} \qquad \text{Eq. A–3}$$

where: t = time
t_{50} = median life time of population
σ = standard deviation of the lognormal distribution

The cumulative distribution function (CDF) is the integrated PDF vs. time, and is given by Equation A-4.

$$\text{CDF} = F(t) = \frac{1}{\sigma\sqrt{2\pi}} \int_0^t \frac{1}{t} \, e^{-\frac{1}{2}\left(\frac{\ln(t) - \ln(t_{50})}{\sigma}\right)^2} dt = \Phi\left\{\frac{\ln\frac{t}{t_{50}}}{\sigma}\right\} \qquad \text{Eq. A–4}$$

where: $\Phi\{\}$ = standard normal distribution function

The median lifetime (t_{50}) is defined as the time at which 50% of the population has failed. This number may be extracted from the life test data using Equation A-5, which is simply the Arrenhius acceleration equation rearranged to yield median life time as a function of operating temperature. By using failure data at elevated operating temperatures, the median life at lower operating temperatures can be estimated.

$$t_2 = t_1 e^{\frac{E_a}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]} \qquad \text{Eq. A–5}$$

where: t_1 = median life time at elevated temperature
T_1 = elevated temperature in °K
E_a = activation energy (slope of Arrenhius curve)
k = Boltzman's constant, 8.6e–5 (eV/°K)
T_2 = operating temperature in °K
t_2 = median life time at operating temperature

The life test data set used to determine E_a comprises a limited number of samples. The students' t distribution may be used to generate upper and lower bounds on its value, based on confidence levels. The derivation of the appropriate limit equations starts with the definition of the T value, shown in Equation A-6.

$$T = \frac{\bar{X} - \mu}{\sigma / \sqrt{N}} = \frac{\ln(t'_m) - \ln(t_m)}{\sigma / \sqrt{N}} \qquad \text{Eq. A–6}$$

where: $\bar{X}$ = measured mean of the data set = $\ln(t_m')$
μ = expected mean of the data set = $\ln(t_m)$
σ = standard deviation of the data set
N = number of samples in the data set

The value of the students' t distribution may also be calculated based on the degrees of freedom (df = N-1) and the confidence level of interest (α). t(df,α) refers to the T value determined using this inverse calculation method. Rearranging Equation A-6, and substituting the new T value yields:

$$\ln(t'_m) = \frac{t(df,\alpha)\sigma}{\sqrt{N}} + \ln(t_m)$$ Eq. A–7

where: $t(df,\alpha)$ = value from students' t distribution
df = degrees of freedom = N–1
α = (1–percent confidence)/2
N = sample size
σ = standard deviation of normal population
t_m = estimated median life value
t_m' = new median life value, based in confidence limits

Solving Equation A-7 for t_m', and substituting single sided t values yields Equations A-8 and A-9. These equations provide upper and lower bounds on the value of median life, based on estimated median life, sample size, and confidence limits required. As a worst–case value the lower limit may be used in reliability calculations.

$$upperlimit = t_m e^{\frac{t(df,\alpha)\sigma}{\sqrt{N}}}$$ Eq. A–8

$$lowerlimit = t_m e^{\frac{-t(df,\alpha)\sigma}{\sqrt{N}}}$$ Eq. A–9

The mean time to failure (MTTF) is defined as the measured operating time of a single piece of equipment divided by the total number of failures of the equipment. It is also used to describe the mean life of a group of devices failing without replacement.

The mean time between failures (MTBF) is defined as the total measured operating time of a population of equipment divided by the total number of repairable failures. This is usually not applied to components since a failed discrete device is not usually repairable.

MTTF is equal to the reciprocal of the instantaneous failure rate. MTTF is not constant with time due to the lognormal failure distribution. However, an approximation for average MTTF, given a median lifetime, is presented in Equation A-10.

$$MTTF_{ave} \cong t_{50}\, e^{\left(\frac{\sigma^2}{2}\right)}$$ Eq. A–10

where: t_{50} = median life time at operating temperature
σ = standard deviation of lognormal distribution

Finally, an average failure rate (λ_{ave}) may be determined by taking the reciprocal of MTTF (Equation A-11). This value is less than the peak instantaneous failure rate, but much larger than the low values found in the early and late life stages. Because standard reliability analyses do not easily handle variable failure rates, this value is often used as an equivalent constant failure rate.

$$\lambda_{ave} = 1/MTTF_{ave}$$ Eq. A–11

It should be noted that σ is not the standard deviation of the population of lifetimes. Rather, it is the standard deviation, in units of lognormal time, for the normal distribution describing the population of logarithmic times to failure. It is sometimes referred to as the shape factor for the lognormal curve and is more a mathematical convenience than a useful tool to predict variations. An approximation for σ, based on life test data, is presented in Equation A-12.

$$\sigma \cong \ln\left(\frac{t_{50}}{t_{16}}\right)$$ Eq. A–12

where: t_{50} = time at which 50% of the population has failed
t_{16} = time at which 16% of the population has failed

Example:

Life test results for a variety of pHEMT devices is reported by Triquint on their website at http://www.triquint.com/MMW. The set of devices used to generate the data includes low power and high power devices. The pertinent information related to these devices is presented in Table A-1. Also included are results of the calculations presented in this Appendix.

Table A-1: Calculated Values Based on LifeTest Data

LifeTest Results Analysis

Parameter	Value	Parameter	Value
Activation Energy (eV)	1.3	sample size N	30
t1 (hrs)	3.44E+03	confidence level (%)	99.00%
T1 (°C)	230	t distribution	2.462
k (eV/°K)	8.61E-05		
shape factor (σ)	0.7		

operating temp (°C)	140		lower limit	upper limit
median life [tm] (hrs)	2.36E+06	--------->	1.73E+06	3.24E+06
median life [tm] (yrs)	2.70E+02	--------->	1.97E+02	3.70E+02
$MTTF_{ave}=tm*exp(\sigma^2/2)$((hrs)	3.02E+06	--------->	2.21E+06	4.14E+06
λ_{ave} (1/$MTTF_{ave}$) (fits)	3.31E+02	--------->	4.53E+02	2.42E+02

mission life (yrs)	f(t)	F(t)	λ (fits)	MTTF(hrs)
1	8.47E-19	5.20E-15	8.47E-10	1.18E+18
2	7.12E-16	8.74E-12	7.12E-07	1.40E+15
3	2.32E-14	4.28E-10	2.32E-05	4.30E+13
4	2.25E-13	5.52E-09	2.25E-04	4.45E+12
5	1.16E-12	3.57E-08	1.16E-03	8.60E+11
6	4.13E-12	1.52E-07	4.13E-03	2.42E+11
7	1.14E-11	4.92E-07	1.14E-02	8.74E+10
8	2.66E-11	1.31E-06	2.66E-02	3.76E+10
9	5.43E-11	3.00E-06	5.43E-02	1.84E+10
10	1.00E-10	6.16E-06	1.00E-01	9.96E+09
20	3.25E-09	3.99E-04	3.25E+00	3.07E+08
30	1.58E-08	2.91E-03	1.58E+01	6.32E+07
40	3.95E-08	9.69E-03	3.99E+01	2.51E+07
50	7.16E-08	2.20E-02	7.32E+01	1.37E+07
60	1.08E-07	3.98E-02	1.12E+02	8.89E+06
70	1.45E-07	6.23E-02	1.55E+02	6.47E+06
80	1.80E-07	8.83E-02	1.97E+02	5.07E+06
90	2.11E-07	1.17E-01	2.39E+02	4.18E+06
100	2.38E-07	1.46E-01	2.79E+02	3.59E+06
150	3.05E-07	2.81E-01	4.24E+02	2.36E+06
200	2.97E-07	3.64E-01	4.67E+02	2.14E+06
300	2.14E-07	3.94E-01	3.54E+02	2.83E+06
400	1.39E-07	3.41E-01	2.10E+02	4.75E+06
500	8.82E-08	2.70E-01	1.21E+02	8.27E+06
600	5.64E-08	2.08E-01	7.13E+01	1.40E+07
700	3.67E-08	1.58E-01	4.36E+01	2.29E+07
800	2.43E-08	1.19E-01	2.76E+01	3.62E+07
900	1.64E-08	9.07E-02	1.81E+01	5.54E+07
1000	1.13E-08	6.92E-02	1.21E+01	8.25E+07

The information extracted from the life test data is presented in the top box, along with desired confidence–level numbers. The left side of the middle box contains the estimated median life at an operating temperature of 140°C, based on Equation A-5. Also included are values for average MTTF and λ. The right side of the middle box presents the upper and lower confidence limits for the same parameters. In this example, a reliability analysis may choose to use a value of 453 fits as a worst–case constant failure rate.

The bottom section of Table A-1 presents the instantaneous failure rates as defined in Equation A-2 as a function of operating time. These values are illustrated graphically in Figure A-1. Note that in the early operating life of the device, the failure rates are quite low. The failure rate increases dramatically until it peaks near the median lifetime. The failure rate then decreases as operating life extends beyond this point. As expected, the peak value of ~467 fits is slightly greater than the estimated average of 331 fits.

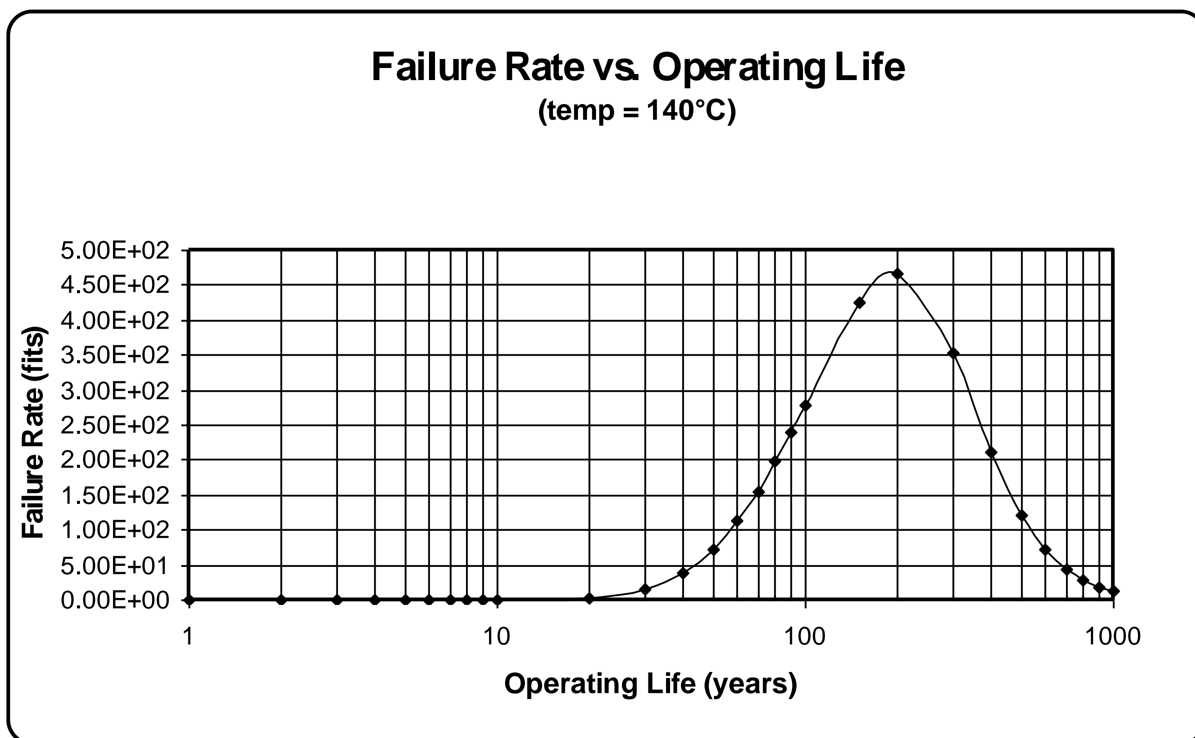

Figure A-1: Instantaneous Failure Rate vs. Operating Time

The purpose of presenting these definitions and analyses is to explain how the failure rates used in this reliability study were generated. Where possible, and for convenience, the average failure rate is used. However, if these numbers yield an unacceptably low probability of success, the values generated using the more accurate method (Equation A-2) may be used.

References:

[1] P. Tobias and D. Trindade, “Applied Reliability”, Van Nostrand Reinhold, New York (1986)