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Step Stress Testing and Determining the Upper Temperature for 3-Temperature Life Testing using the AARTS System

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Accel-RF Corporation specializes in the design, development, manufacture, and sales of accelerated life-test/burn-in test systems for RF and Microwave semiconductor devices. This white paper describes technical information related to the AARTS Hardware. For more information contact:

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1 Overview

This document describes a methodology to implement step-stress testing using the Accel-RF AARTS life test system. Step-stress testing is performed for a variety of reasons, including: shortening overall life test duration times; defining an appropriate upper temperature limit for 3-temperature life testing; and providing a quick method for monitoring process control metrics.

Failure mechanisms in semiconductor devices may be accelerated by "stressing" the parts, generally utilizing increased DC stimulus, RF stimulus, and/or temperature stimulus. Step stressing implies that one stimulus is increased in "steps" while monitoring overall device performance for some prescribed period of time.

A number of degradation models have been developed around step-stress paradigms for determining device lifetimes and failure rates [1, 2]. Dynamic modeling, using maximum likelihood estimators, can become quite complex. Abbreviated techniques have been developed to enhance model determination while maintaining model simplicity [2, 3].

A common standard utilized by many companies for determining and reporting failure-rate information is the JEDEC JEP118 document [4]. This document defines a methodology for determining failure-rate information using 3-temperature test acceleration. The basic concept is to run samples of devices at three different temperatures and determine times to failure for a specific performance parameter. It is important that the failures at all temperatures be caused by the same mechanism (e.g. gate sinking). Step-stress tests are employed to ascertain an appropriate upper limit for temperature acceleration, which minimizes overall test times while avoiding deleterious failure effects that are not related to "common" mechanisms at each temperature.

1.1 Background

When performing 3-temperature life tests, it is important to choose appropriate temperatures that minimize test time and maximize model confidence. While test times decrease with increasing test temperature, it is possible to induce multiple degradation effects if the temperature is too high, thus voiding the degradation model validity. So what is the appropriate upper temperature limit? To answer this question it is helpful to review some useful equations.

Typical semiconductor degradation mechanisms may be described using the well-known Lognormal Distribution model [5]. This model states that failures will be normally distributed as a function of log time. Hence, if failure times (related to a common failure mechanism) are plotted on a normalized scale vs. the logarithm of time, they will appear as a straight line – as illustrated in Figure 1.

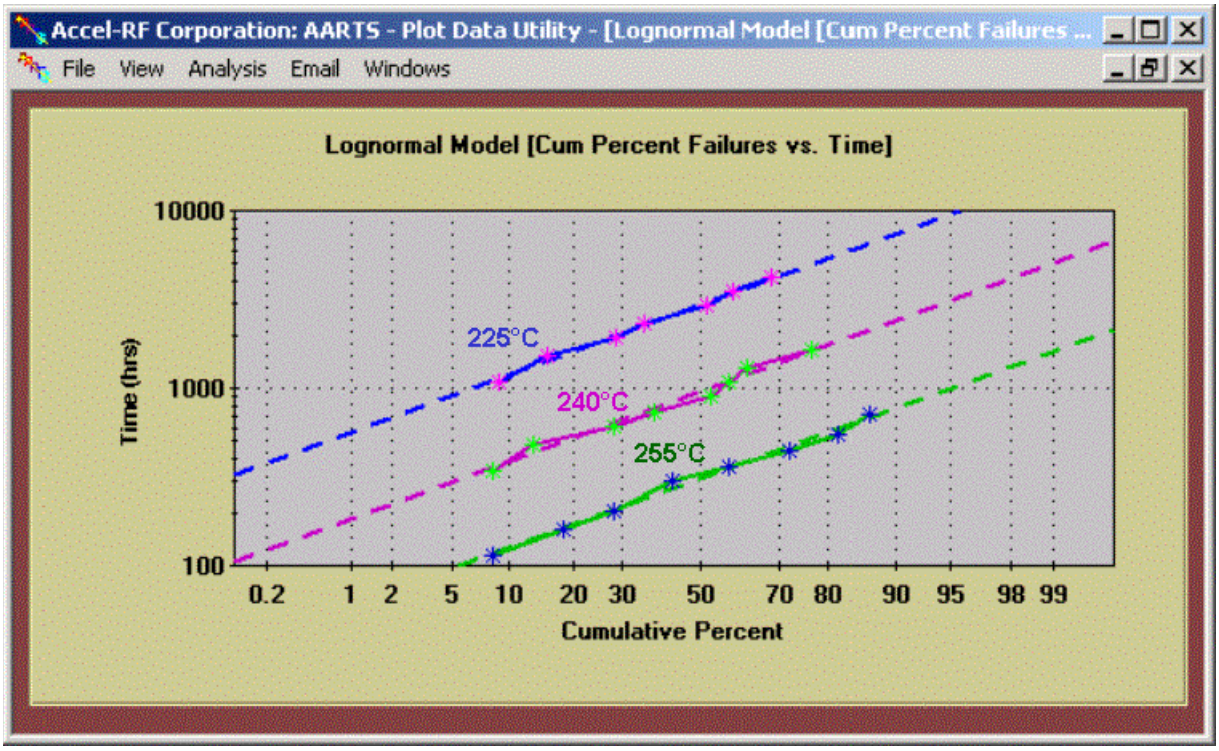
Arrhenius showed that chemical reactions, such as though involved in most semiconductor failure mechanisms, could be accelerated with temperature. Equation 1 presents the well known Arrhenius equation as applied to the median lifetime of device failures.

$$T_{50} = A e^{\left[\frac{-E_a}{kT}\right]}$$

Equation 1

where:
T_{50} = median lifetime
A = a proportional multiplier, which can be a function of temperature
Ea = activation energy
k = Boltzman's constant, 8.6 x 10–5 (eV / °K)
T = temperature (°K)

Figure 1: Lognormal Model



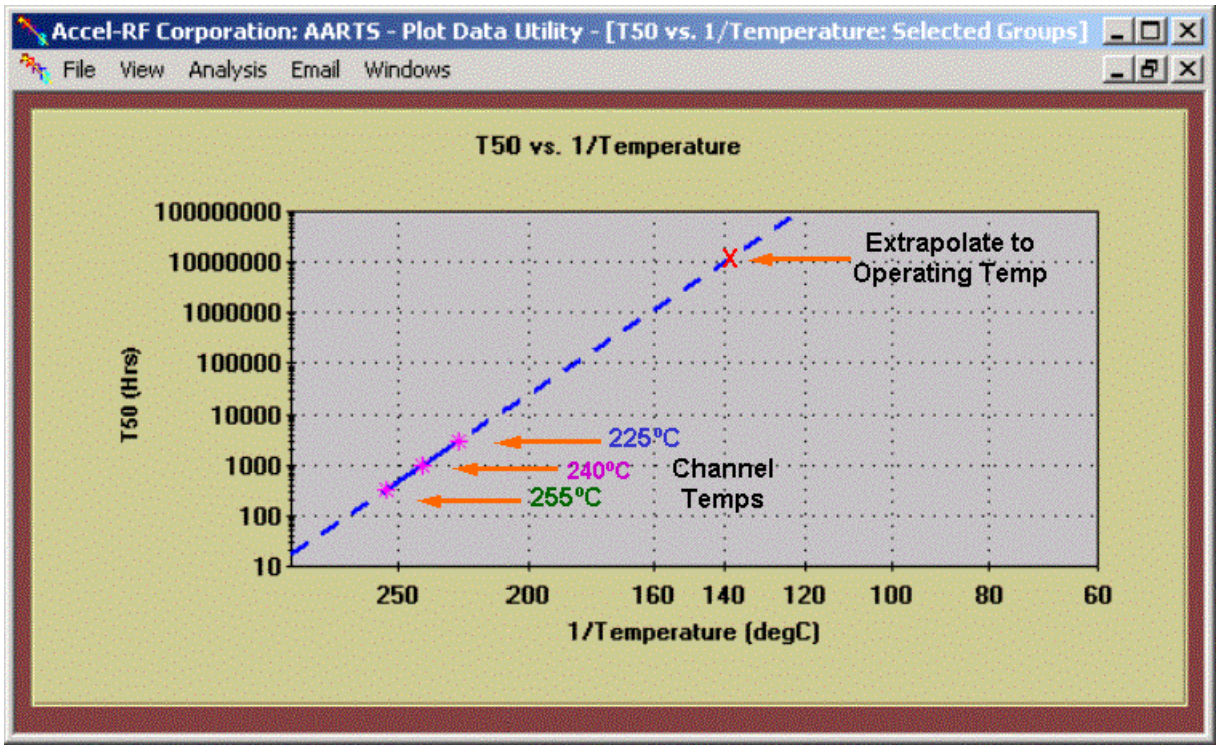
The Arrhenius equation states that as temperature increases, times to failure decrease. The three different sets of data in Figure 1 illustrate such as example. The straight-line-fit slope of the Lognormal CDF is called the shape factor. The intercept is equal to the median time to failure, or T_{50} point. If the failure mechanisms are well behaved, with respect to the model definition, the slopes of the normalized data will all be equal, with different intercept (T_{50}) points. Differing slopes of the straight-line fits imply a breakdown in the Arrhenius assumptions; and hence, could suggest multiple failure mechanisms.

The Arrhenius relationship (Equation 1) may be rearranged to yield Equation 2. Note that this is a linear equation of the logarithm of Time vs. 1/Temperature. Hence, if the T_{50} points are plotted on such a normalized scale, the result will yield a straight line, as shown in Figure 2. This curve is useful for extracting the exponential constant Ea, also known as Activation Energy. This constant is a key factor in describing the device reliability, and may be extracted per Equation 3 by multiplying the slope of the straight-line by Boltzman's constant, k.

$$\ln(T_{50}) = \ln(A) - \frac{1}{kT} E_a \qquad \textbf{Equation 2}$$

$$E_a = \frac{\left[\ln(A) - \ln(T_{50})\right]}{1/T} k \qquad \textbf{Equation 3}$$

Figure 2: Arrhenius Model



Given at least one time to failure point and activation energy, the time to failure at any other point may extrapolated using Equation 4. Note that time t_2 represents the time to median failure at temperature T_2. The time t_r is the median time to failure at a reference temperature T_r.

$$t_2 = t_r e^{\frac{E_a}{k}\left[\frac{1}{T_2} - \frac{1}{T_r}\right]}$$

Equation 4

By expressing T_2 in terms of a temperature difference relative to the reference temperature T_r, Equation 4 may be rearranged to yield Equation 5. Note that the ratio of time-to-failure (t_2 / t_r) is a function of Ea, reference temperature (T_r), and delta temperature ($\Delta T = T_2 - T_r$). Equation 5 provides a convenient way to evaluate the step-stress time-expansion effects.

$$\frac{t_2}{t_r} = e^{-\frac{E_a}{kT_r}\left[\frac{\Delta T}{T_r + \Delta T}\right]}$$

Equation 5

1.2 Step-Stress Methodology

How does the background information developed in Section 1.1 impact the methodology for life testing? First, as noted earlier, it is desirable for the lowest temperature to yield test times that are short enough to avoid extended test times (e.g. years). Yet, the highest temperature should not yield such short times that data statistics suffer or that multiple failure mechanisms are induced.

Three temperatures are typically utilized to minimize the unavoidable extrapolation errors induced in 2-point analysis. By using more than two temperatures a curve-fitting process may be utilized to essentially minimize measurement and some test errors without generating excessive test times. Additional temperatures would be useful, but again would extend test time. Further, there should exist a minimum separation between temperatures to avoid analysis computational overlap (JEP118 suggests a 15ºC separation between test temperatures).

A primary concern regarding any new technology is determining the correct upper temperature for the 3-temperature life test. If historical data exists for the technology of interest, it could be used as a first-pass assumption for the upper temperature. If not, JEP118 suggests a temperature step-stress paradigm to define the proper temperature. In this method, six devices are set on test at a surface temperature of 150ºC. After at least 24 hours, the surface temperature is increased by 25ºC. The surface temperature is repeatedly increased in equal time duration steps until at least 50% of the devices have failed. Although 24 hours is a recommended minimum, it may not yield enough performance degradation to confidently determine when devices have failed, particularly if the devices exhibit a very low Ea. Hence, many people prefer to use a longer 72-hour duration period. The maximum 3-temperature life test temperature is then defined as 20ºC below the step-stress interval in which the 50% failures occur. Finally, the other two temperatures would be progressively lowered by 15ºC.

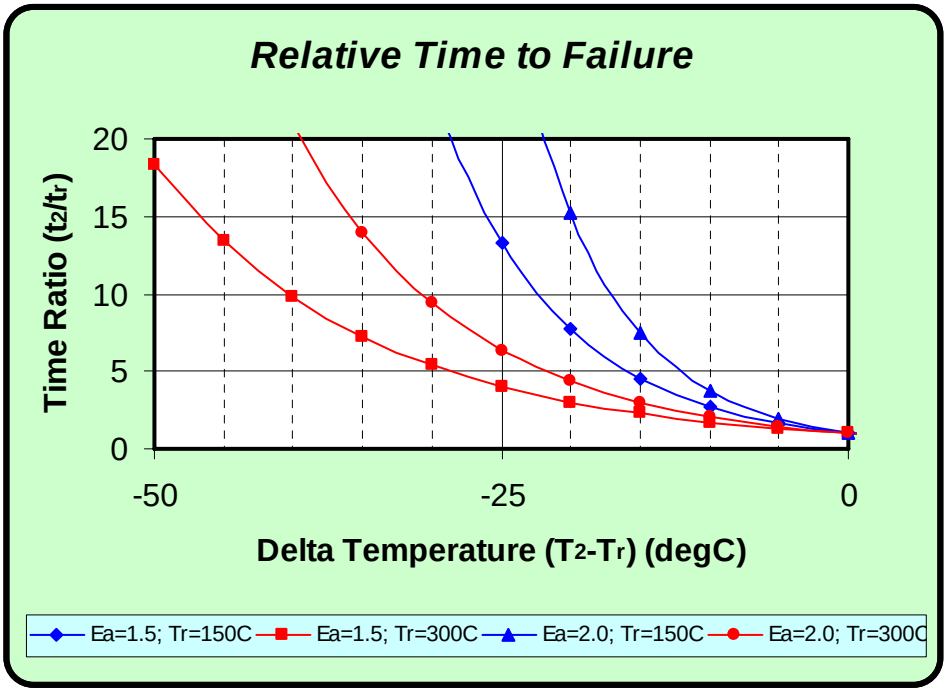
Lets consider the repercussions of these testing paradigms. A convenient approach to analyzing the paradigm assumptions is to plot Equation 5 for some representative worst-case scenarios as shown in Figure 3, with reasonable values of Ea = 1.5 and 2.0, and reference channel temperatures values of Tr = 150ºC and 300ºC. The blue lines represent results created at the lower temperature and the red lines show the higher-temperature results.

Again, the JEP118 standard recommends starting the step-stress intervals at 150ºC and incrementing in 25ºC steps until 50% failures occur. The channel temperature is of course, by definition, higher than the surface temperature and is a function of power dissipation in the device. To make things convenient, it is common to run the step tests at surface-temperature intervals of 150ºC to 250ºC in 25ºC steps. The AARTS system is designed to facilitate this testing paradigm using the LifeTest AutoSequence [6] features.

Considering that parameters such as device gain or RF output power are functions of temperature, a key question arises of how to evaluate failures. A common practice is to evaluate degradation independently at each temperature interval. For instance, the performance of Gm might be analyzed as a percentage change relative to the first measurement at the new temperature interval. The analysis routines in the AARTS system have been designed to efficiently extract data in this format.

What about cumulative degradation effects of performing tests in this fashion? Referring to Figure 3, note that the recommended step size of 25ºC at the lower reference temperature of 150ºC (blues lines) yields a time to failure expansion ratio >10. Hence, the effects of the lower-temperature dwell times are minimal with regard to the next step's degradation. At 300ºC channel temperature the expansion is <5 for an Ea = 1.5. This would result in some noticeable impact of aggregate failure degradation caused by the previous temperature steps, but still lends itself to effectively evaluating device performance degradation at each step as independent events.

Figure 3: Relative Times to Failure vs. Delta Temperature



Clearly, a tradeoff exists between temperature step-size/dwell-time and determining performance failure. As discussed above the step size of 25ºC has been chosen as a minimum increment to make independent evaluation at each new temperature reasonably valid. Greater increments could be chosen to maximize the time-expansion characteristics even further. Generally, the recommended 25ºC increment is considered acceptable.

Dwell time is the next factor to determine. The amount of time needed at each temperature is very dependent on the device itself. A device exhibiting very low activation energy will take longer to degrade than one with high Ea. If dwell time is too short there may not be enough time for degradation to be evident at the highest temperature. In the JEP118 document, a minimum interval of 24 hours is recommended. This value was somewhat arbitrarily chosen to support older manual systems where a human had to check on the device performance once a day. Although 24 hours may work well for devices with Ea = 2, it could be too short for devices with an Ea = 1.5. Practically, a dwell-time value of 72 hours per step works well for most microwave devices.

What type and how often should data be taken? Because the AARTS system is fully automated, there is no need to accommodate measurement times to human convenience. Continuous monitoring and storage of static performance data is performed using the LifeTest software during each temperature interval. However, it may be desirable to perform more accurate, or even pulsed-sweep, analyses using an optional Semiconductor Parameter Analyzer (SPA). The AARTS system supports such testing paradigms in both hardware and software. In fact, SPA and RF gain-compression sweeps may be performed at any time interval desired. Note that some small (but measurable) time is required to setup and perform these sweeps, during which additional elapsed time is accrued but not monitored. A good compromise is to perform special tests at a minimum interval of 8 hours.

Several questions commonly arise at this point. First, what type of stress stimulus should be presumed? That depends on what failure criteria is most critical. Some argue that a constant (active) bias should be used to maintain a constant power dissipation in the device, due to the fact that t_{jc} (the case-to-channel thermal resistance) is not truly constant as a function of power dissipation, and is also a function of

surface temperature. Maintaining an active DC bias may be fine for a DC-only stimulus paradigm, but if RF is also applied the system would have to take into account the change in RF power levels (i.e. gain and power output performance affects total power dissipation). Fortunately, the AARTS system offers the option to maintain a constant RF output (or input) power by continually adjusting the input power.

The disadvantage of maintaining constant power dissipation is that drain- or collector-current (or RF output power) are key parameters of interest with regard to device degradation. An alternative approach is to maintain constant channel temperature by dynamically adjusting the surface temperature, thus alleviating the requirement of operating under an active-bias scenario. In this mode, the AARTS system monitors device power dissipation and dynamically adjusts the surface temperature, based on surface-to-channel temperature gradient calculations, to maintain constant channel temperature.

An interesting related, and very pertinent, point may be observed in the data shown in Figure 3. Consider the worst-case condition of Ea = 1.5 at Tr = 150ºC. As shown, an error in channel temperature of 5ºC yields a relative time difference of 1.93. Further, a 10ºC error yields a factor of 3.78. At 300ºC, a 10ºC error results in a time-to-failure error of 2. The point to note is that a fairly small change (or error) in channel temperature can have a significant effect on the results, with the magnitude magnified at lower temperature and higher Ea. This could be important for the proper choice of bias conditions, depending on the confidence of the device thermal models and resultant surface-to-channel temperature gradients.

The JEP118 standard suggests selecting a maximum life test temperature 20ºC below the step-stress temperature at which 50% failures occur. That amount of temperature decrease, even at a modest maximum channel temperature of 250ºC and Ea = 1.5, yields a time expansion of 3.7. At a test dwell time of 72 hours, this would yield an expected maximum-temperature test time of 266 hours (11 days).

JEP118 also recommends separating the test temperatures of the 3-temperature life test by 15ºC to avoid statistical measurement errors that could contribute to significant errors in the Arrhenius results. This paradigm results in a 30ºC difference between highest and lowest temperature. Assuming a new reference maximum temperature of 230ºC and Ea of 1.5, the time expansion to 200ºC is 9; hence, the life test time would stretch to over 2,394 hours, or almost 100 days. This would be considered a reasonable time to yield 3-temperature life test results.

2 Implementing Step-Stress Methodology Using the AARTS System

Historically, step-stress testing using the paradigm discussed above employed a very manual process. For instance, once a day the operator might come to the system and shut the stress bias off to run a Semiconductor Parameter Analyzer (SPA) sweep or RF power sweep, from which accurate degradation information related to a variety of parameters may be ascertained. At best, this yields limited data points for each step. At worst, it requires a significant amount of user interaction to obtain data and often involves moving the device/fixture to a different location, potentially leading to mechanical or ESD damage due to handling. Once the data is captured, a further amount of data processing is required to identify failures.

The AARTS system has incorporated the necessary hardware and software tools to significantly reduce user-interaction time, acquire additional data at shorter intervals spaced regularly apart in time, and extract the information needed to identify failures.

The system utilizes its AutoSequence operational mode to setup and control a variety of stress conditions. Under this paradigm, the user defines a set of stimuli (RF, DC, and thermal) for each time interval. The step duration (dwell time) is also defined by the user. Once launched, all steps in the sequence are performed automatically. The user need only review the results to determine the appropriate upper temperature limits, as defined in JEP118.

An example of a flexible test-sequence paradigm, as implemented in the LifeTest software is presented in Figure 4. The example shows a method whereby a SPA sweep occurs every 8 hours, with the stress stimulus conditions presented for the 8-hour duration. The "For" loop causes the interval to be repeated 9 times, yielding a total of 72 hours at each temperature. The additional SPA sweep (as shown in step 5) is included to assure a final sweep is performed after the dwell duration time. Note that different stimulus states may be defined for each temperature; however, if a common definition is used, the stimulus definition may be ignored in the sequence setup.

Figure 4: Test Sequence Definition

```
1;      For i = 1 to 9
2;        SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 150.00
3;        Stress Test; Duration = 000  08:00:00; Temp = 150.00; Stimulus File = DEFAULT & "STIMULUS.150"
4;      Next
5;      SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 150.00

6;      For i = 1 to 9
7;        SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 175.00
8;        Stress Test; Duration = 000  08:00:00; Temp = 175.00; Stimulus File = DEFAULT & "STIMULUS.175"
9;      Next
10;     SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 175.00

11;     For i = 1 to 9
12;       SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 200.00
13;       Stress Test; Duration = 000  08:00:00; Temp = 200.00; Stimulus File = DEFAULT & "STIMULUS.200"
14;     Next
15;     SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 200.00

16;     For i = 1 to 9
17;       SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 225.00
18;       Stress Test; Duration = 000  08:00:00; Temp = 225.00; Stimulus File = DEFAULT & "STIMULUS.225"
19;     Next
20;     SPA Test; Definition File = \SPA Idss Sweep.SPA; Temp = 225.00
```

Two common problems exist in life test systems when trying to run special tests, such as SPA or gain-compression sweeps. First, maintaining coherent data results are often difficult when intermediate interruptions occur. Consider that during a stress duration device degradation occurs. When the test is interrupted and potentially even lowered in temperature to a control temperature, such as 100ºC, returning to the stress conditions that were previously in place may not be trivial. Second, device annealing is sometimes evident when bias and temperature are removed for a significant amount of time. Hence, when the stress interval is resumed, device performance jumps are noticeable.

The AARTS system is designed to minimize these effects. Several operational modes are available to automate device setup so that device bias and temperature startups are very repeatable. Further, by performing the special tests at temperature and in the same physical locations (i.e. not having to remove the fixture to a different test location), the system minimizes down time between stress intervals, thus preventing significant annealing effects. Finally, because each devices DC, RF, and thermal stimuli are controlled independently, adding and removing a device-under-test is not dependent on the state of other devices.

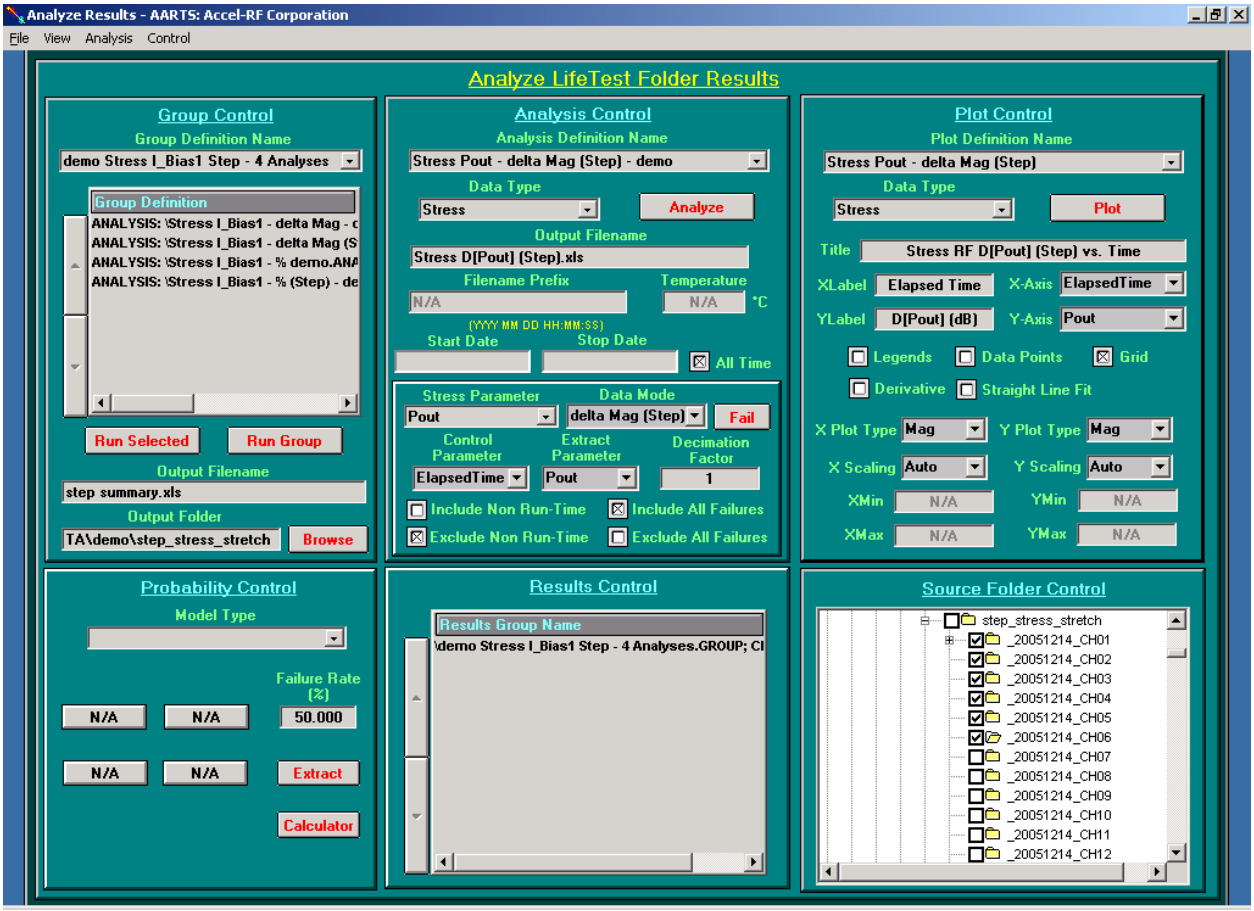
3 Analyzing Step-Stress Data Using the AARTS System

Once the data is acquired, it must be analyzed. The AARTS Aggregate Analysis tools are designed to provide the user with a plethora of options for analyzing data. A screen shot of the LifeTest analysis tools interface is presented in Figure 5. It is designed to support generic creation of any number of analyses against user-defined failure criteria. Data could subsequently be analyzed independently or as an aggregate batch.

To use the Aggregate Analysis tools, the user creates a library of analysis and related plot definitions. The data extraction-mode options offer five processing algorithms: 1) “Mag” - magnitude only; 2) “delta Mag” – magnitude information normalized to the first data point; 3) “%” – data normalized to the first point, returned in percentage change format; 4) “delta Mag (Step)” – data normalized to the first point in each new temperature interval; and 5) “% (Step)” – data normalized to the beginning value in each temperature step, returned in percentage change format.

A variety of optional data extraction algorithms are available, including derivative information at specific bias points and peak-search derivatives for tracking peak changes. Four types of data may be analyzed: 1) stress; 2) transistor staircase sweep (single sweep); 3) transistor family of curves sweeps; and 4) gain-compression sweeps.

Figure 5: Analyze Folder Results Form



Once a library of analyses have been defined, the user creates a set of groups, comprised of one or more analyses and associated plot definitions, a set of associated "tagged" folders that contain the data to be processed, and information regarding where the summarized results are to be placed. This makes periodically updating run results as simple as selecting a single group definition and clicking "Run Group".

By judicious creation of group definitions, the user can quickly create multiple temperature run information and analyze the data against several failure models, such as Lognormal and Weibull (please refer to the AARTS software manual to further information on the statistical modeling options).

For the purpose of analyzing step-stress data, consider the example data set presented in the following plots. Figure 6 shows the step-stress temperature intervals as a function of accrued elapsed time. Note that the dwell time at each temperature is 72 hours. The cumulative magnitude degradation of drain current is shown in Figure 7. Figure 8 shows the same data returns in percentage change format using the "% (Step)" option. Hence, the data is normalized to the first point in each temperature interval. In this example, the 20% failure criteria was not quite attained in a specific temperature frame, but clearly the devices are exhibiting significant degradation in the last two intervals. Given the cumulative effects, a conservative estimate of the proper temperature would be 250ºC. Hence, the upper temperature for the 3-temperature life test would be 230ºC.

Figure 6: Step Stress Temperature

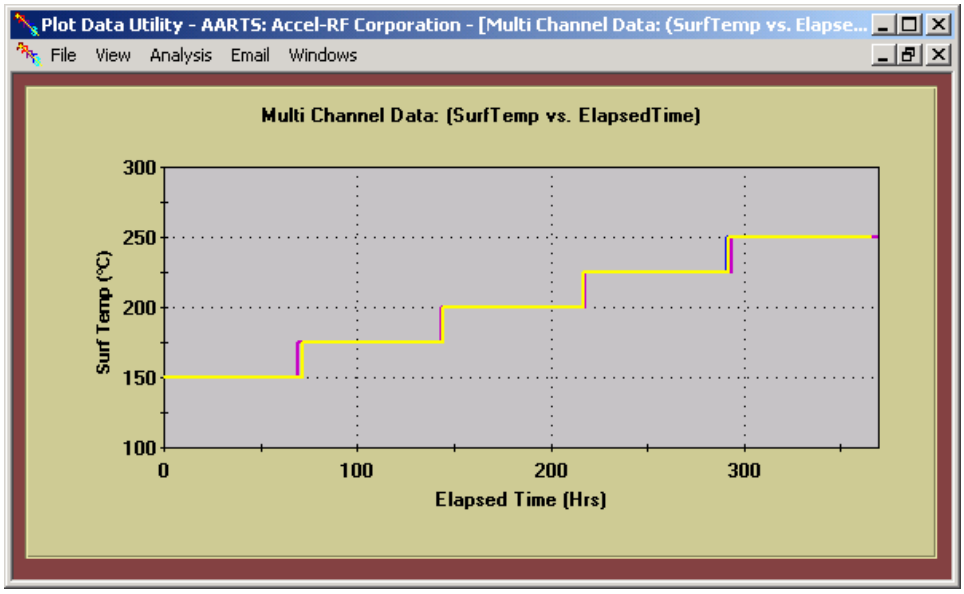


Figure 7: Step Stress Ids Degradation

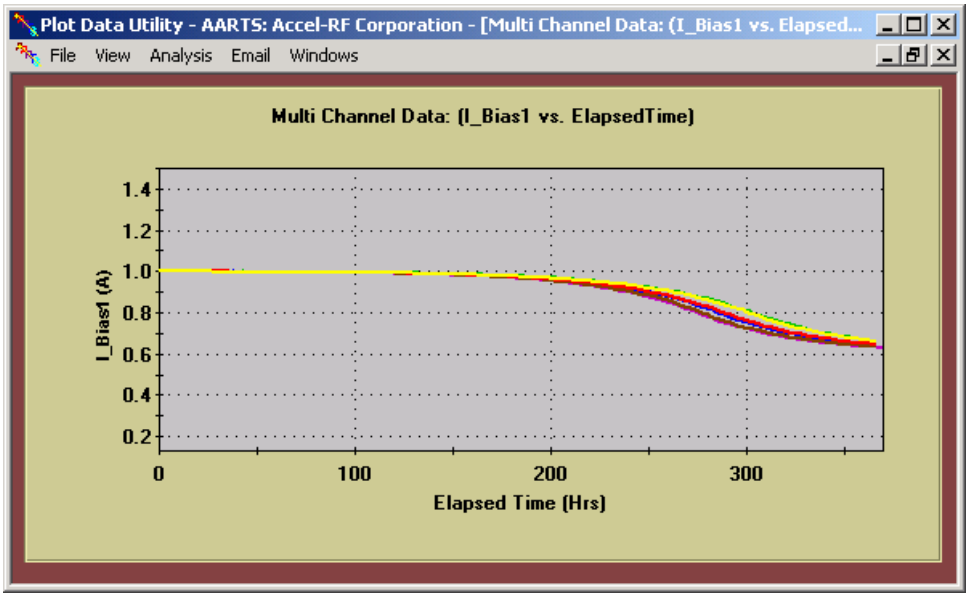
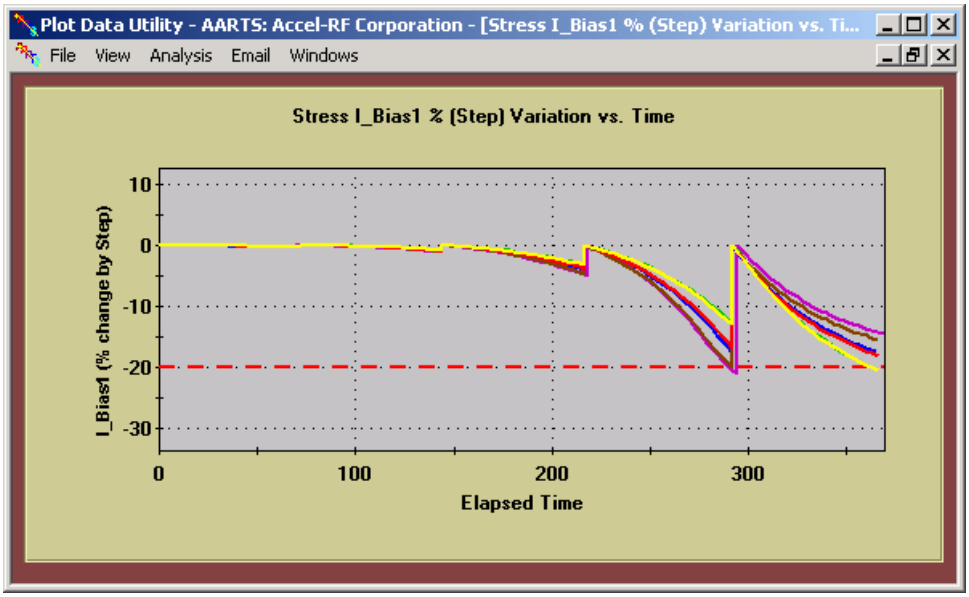


Figure 8: Step Stress Ids % Degradation (Step)



A similar example using RF output power degradation, reported in delta dB format is shown in Figure 9 and Figure 10. Again, any number of extraction analyses may be defined and analyzed using the AARTS Aggregate Analysis Tools.

Figure 9: Step Stress RF Pout Degradation

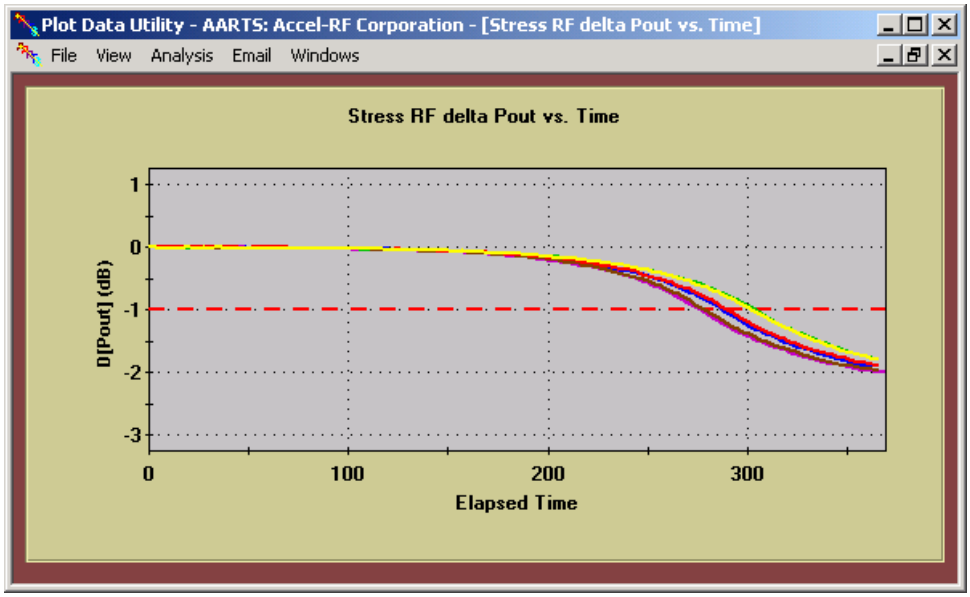
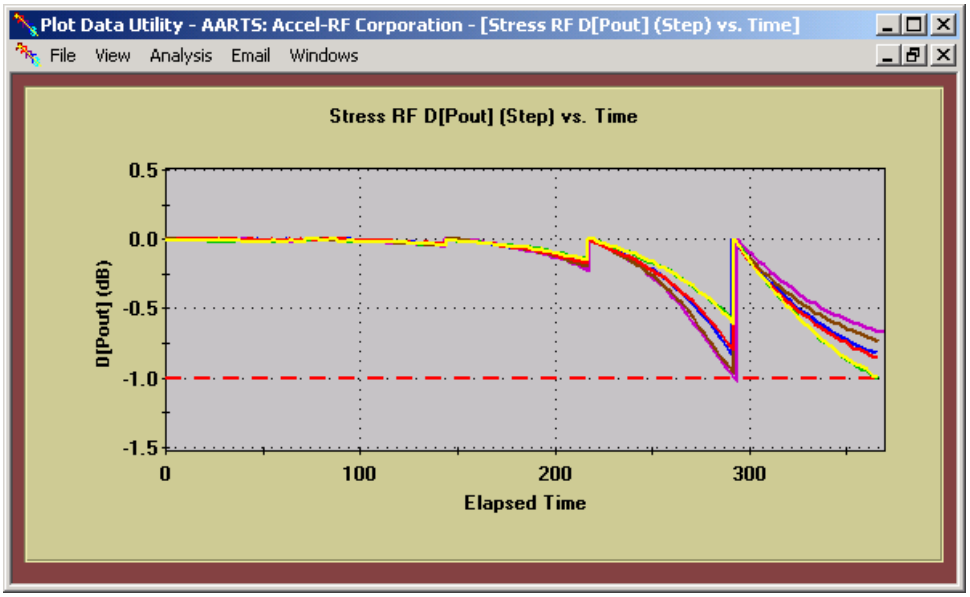


Figure 10: Step Stress Delta RF Pout Degradation (Step)



4 Summary

Step-stress testing is useful for a variety of purposes. Specifically, the JEDEC JEP118 standard suggests a methodology for determining the upper temperature in a 3-temperature life test. Further, step-stress testing may be used to develop accelerated life testing algorithms.

The AARTS system is designed to support easy implementation of very generic step-stress stimuli, including DC and RF bias stress variations as well as temperature stress variations. The fact that any number of test sequences and stimulus defintions may be arbitrarily defined opens a world of test methodologies previously unavailable.

The Aggregate Analysis tools offer a flexible way to extract and analyze step-stress data results. The AARTS system simplifies the task of data acquisition and analysis so that the reliability engineer can focus on the real issues of concern – understanding and fixing problems in the device physics and manufacturing processes.

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1. Gaw, C; Arnold, T.; Martin R.; Zhang, I.;, Zupac D.; "*Evaluation of SiGe:C HBT Intrinsic Reliability using Coventional & Step Stress Methodologies"*, Reliability of Compound Semiconductor Workshop, CSMAX, 2005.

2. Tobias, P.; Trindade, D.; "*Applied Reliability"*; Chapman & Hall, ISBN 0-442-00469-9; pg 166-218.

3 . King, J.; *Probability Charts for Decision Making*; Technical and Engineering Aids for Management; ISBN 0-8311-1023-6; 1981.

4. JEDEC, JEP118; "*Guidelines for GaAs MMIC and FET Life Testing"*; January, 1993.

5. Kielpinski, T.; Nelson, W.; "*Optimum Censored Accelerated Life-Tests For The Normal and Lognormal Life Distributions"*, IEEE Transactions on Reliability, Vol. R-24, pp310-320.

6. Sanderlin, D.; "*AARTS Software Manual, Rev E*"; Accel-RF; July , 2005.