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RF Matching Circuit Design Methodology for RF Life Testing using the AARTS System

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Accel-RF Corporation specializes in the design, development, manufacture, and sales of accelerated life-test/burn-in test systems for RF and Microwave semiconductor devices. This white paper describes technical information related to the AARTS Hardware. For more information contact:

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1 Overview

This document describes a methodology to create device-under-test (DUT) matching structures for use in the AARTS RF life testing station. This is important to assure unconditional stability and optimize RF performance so that device degradation may be accurately assessed. Parameters such as PAE and RF output power (Pout) are important criteria for system level performance and reliability prediction. For those devices that are internally matched, such as a MMIC, providing a 50-Ω load may be sufficient. However, for discrete devices, or partially matched devices, additional matching elements are required to yield peak performance.

While standard matching techniques may be used to create stand-alone bench circuits, or even modular products, there are some issues related to life-testing that are unique. In particular, the DUT must be heated to very high temperatures to accelerate the aging effects. 200°C to 250°C device surface temperatures are not uncommon. However, elements of the matching structures, such as resistors, capacitors, and substrate dielectric constant are sensitive to temperature, which may even exceed acceptable operating limitiations. For instance, standard 0805- and 1206-resistor power dissipation limits are derated to 0W above 150°C.

Ideally, the life test RF fixture would provide a “point” heat source right at the DUT mounting surface, and not immediately outside of the DUT periphery. However, this is unrealistic. First, there must be some mechanism to ascertain the surface temperature by mounting a probe of some sort (e.g. thermistor, thermocouple, etc..) very near the surface of interest. This probe must not affect the ability of the heater to appear as an “infinite” heat sink. Further, it is difficult to accurately control the temperature of such a small thermal mass. Finally, in order to accommodate a variety of device structure sizes, and/or to facilitate quick release mechanisms, some physical headroom is required.

All of these factors contribute to the difficulty of creating a suitable matching circuits for RF life testing. Accel-RF has performed RF life testing for many years, and has developed some understanding of the tradeoffs and limitations for obtaining meaningful reliability data under RF stimulus. Of course, each new device is different, but the following methodology that has proven successful in many applications.

2 Background

Accel-RF AARTS stations support independent thermal, DC, and RF stimulus to each DUT position. RF power is monitored using a simple scalar calibration approach of applying a reference calibration factor (see for descriptions of how the calibration approaches work). An example of a typical AARTS RF test fixture is presented in Figure 1. The center gold-plated brass block provides excellent thermal mass and is where the DUT is mounted. The outer area is thermally isolated from the heater element and remains relatively cool. A small air-gap must be bridged for the RF to perform optimally. A proprietary coplanar transition provides excellent RF performance up to ~20GHz, while maintaining good thermal isolation. Finally, as seen in the lower area of the picture, a quick-release clamping mechanism eliminates the need for welded interconnect straps or wire bonds to make the RF interface.

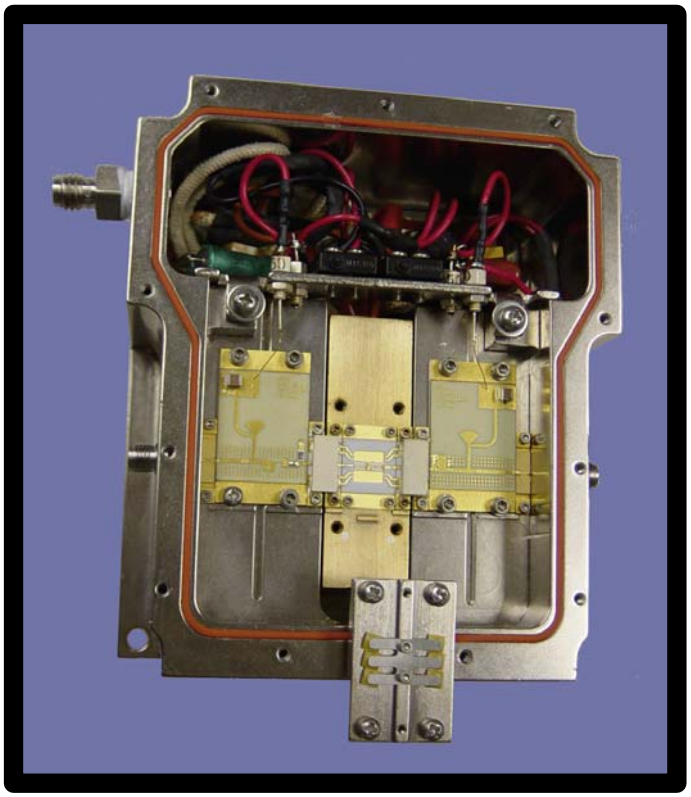
As illustrated in the picture, an unavoidable distance exists between the DUT and the input/output matching circuits. This becomes problematic when the extra line length is sizable in comparison to a wavelength. At microwave frequencies, this length is indeed very critical. Under ideal conditions, designing a broadband matching structure can be challenging; including the additional phase rotation of the interface lines to the matching structures makes the task even harder.

Several assumptions make the task manageable. First, for life test purposes, broadband performance is not required since RF power and gain measurements are all made on a CW basis. Second, relative

power changes, particularly output power, are the critical factors of interest. Lower gain caused by matching circuit realities is less important.

Absolute power can be important for determining total power dissipation in the device. It should be noted that the AARTS station does not perform full error correction, impedance matching is moderately important. This is particularly important on the input side because it affects the amount of power delivered to the device. Large reflections can cause measurement accuracy errors. Fortunately, accuracy of input errors are significantly less important than knowledge of power extracted from the device. This is because the total power dissipation in the device defines the temperature rise from the surface to device channel (or junction), and typical device gain makes the input power an order of magnitude less important.

Figure 1: RF Test Fixture



3 Design Methodology

Given the physical realities of heating the device and routing RF to and from the outside world, what is the proper technique to yield best performance? The answer depends on the device being measured. For instance, a power amplifier provides the best PAE and output power performance when the output load match is somewhat different than the ideal conjugate match. This is, of course, achieved at the expense of optimal output return loss (S22, also related to VSWR). In the case of a low-noise amplifier, the input match is more critical, and again not equal to the conjugate values.

These optimal load impedances are often referred to as gamma loads. The optimal loads are determined either by modeling the device using linear and/or nonlinear simulators and analytically optimizing performance, or by physical measurement techniques using load-pull systems, in which a scattering of impedances are presented to the device and resulting performance noted. In order to simplify the measurement process, the load-pull system may present a fixed load of 50-Ω to the complimentary port, while presenting an array of impedances to the port of interest. However, when the pulling process is automated, a complete set of pulling results may be obtained by performing the full load sweep for each of a wide range of input impedances. It should be noted that the impact of the opposite port load will be of second order as long as the S12 factor is very small, which is generally true for the active gain devices typically being life tested. This fact is useful for our purposes because of the following considerations.

Perhaps the overriding issue in designing the matching circuit is stability. If the device breaks into oscillation, not only do the measurements become corrupted, but the stresses on the device can be high enough to dramatically affect the failure mechanisms being analyzed, and hence irreducibly change the reliability statistics. Hence, it is imperative that the device be unconditionally stable over the full bandwidth at which gain exists. For microwave devices, this involves evaluating the S-Parameters over a typical bandwidth of ~45MHz to 20GHz. Millimeter-wave devices would need to extend to even higher frequencies.

There are several ways to achieve unconditional stability. Designing for stability is conveniently visualized using the Smith chart. Stability circles indicate those impedances that, if presented to the device under the right conditions, might result in oscillation. If the matching elements could be placed right at the device terminals, purely reactive matching elements could have a chance of providing the required stability performance. Unfortunately, with the additional phase rotation caused by the transitions to the outer area, this is not feasible.

Practically, employing series- and shunt-resistance on the input and/or output is the only realistic way to push all stability circles outside of the real resistance part of the Smith chart. By definition this means there is some loss associated with stabilization. For power amplifiers, this additional loss is best placed before the amplifier, since the output power may be too large for the resistors to handle. For low-noise amplifiers the resistors might preferably be placed on the output to yield optimum noise performance. In either case, the losses will need to be estimated and included in the RF calibration process to yield proper device input/output level determination [xxx].

Once the output (or input) load is created, and the opposite port matched to force unconditional stability, a conjugate matching structure should be employed to maximize return losses. This yields a reasonable compromise between RF gain and power performance, stability, and system performance.

To summarize, the design steps are:

1. Decide on a device bias point, perhaps based on a series of load pull results. Identify the proper gamma load for input or output match as required.

2. Design the proper load matching circuits to present the desired gamma load impedance, keeping in mind the power and current ratings of the various matching elements. Note that the load match must include the transmission line elements required to reach the outer block area from the device.

3. Looking at the stability circle locations, as referenced at the input/output starting reference planes, decide upon an architecture that yields unconditional stability at all frequencies (note: series and shunt resistive elements offer the most flexible approach).

4. Design a conjugate match on the opposite side of the gamma load port to maximize return loss and gain for the resultant circuit. If the conjugate match does not yield reasonable impedance match (R.L. > 10dB) on the gamma load port, some performance tradeoff may be needed to avoid excessive

system performance pulling. Historically, this has not been required. Unless the optimal gamma load is extremely far away from 50Ω, following the above design methodology yields reasonable impedance matching performance on both ports. Be sure to include DC blocking capacitors in the series RF line as the source and load impedances extend to DC.

5. Add in the required bias choke elements on input and output ports. A common approach is to use quarter-wave radial stubs on the end of a quarter-wave transformer to yield a high-impedance choke at the RF signal line. If inductive lumped elements are preferred, be sure the current carrying capacity of the choke is adequate.

6. Estimate the loss from fixture input/output to the device terminals. This can be done by modeling, or by inserting a through line in place of the DUT and applying an appropriate loss distribution percentage to the total measured insertion loss. These losses should be inserted into the RF calibration factors (see [xx] for a description of how to fine tune the calibration factors).

4 Matching Circuit Design Example

This section presents a matching circuit design example using the methodology described in Section 3. Microwave Office (MWO) was used for linear simulation and design optimization. The device being tested was an X-Band GaN power transistor biased at Vds=+20.0 V, Ids=80.9 mA, Vgs= 2.495 V, and Igs= 0.0 mA. The expected output power was xxx dBm.

4.1 Step 1 – Identify Desired Gamma Load

The output gamma load was determined using load pull techniques to be 0.561 $\angle$ 38.8 at 10GHz, which maximized RF Pout. This is used as the design goal, with some flexibility given to the exact target frequency at which the tests are to be performed.

4.2 Step 2 – Design the Gamma Load Output Matching Circuit

To design a matching circuit that provides the desired load to the device terminals, a model must be created that accounts for the transmission line effects of the transition elements between the device and the output matching circuit elements. First, we will consider a model of the entire inner area of the fixture, which supports the high-temperature operation. Then, we will break the model into its input and output components to design the appropriate matching circuits.

Referring to Figure 1, the key elements to model are the input and output coplanar transitions that span the air gap from the outside area to the heated block; the input transitions that comprise the carrier assembly (in this case a Stratedge LCC package); 50-W microstrip transmission lines which route the RF signal to the edges of the device; and the wire bonds that connect these elements.

The MWO model for the inner block area is shown in Figure 2. The coplanar transition model is derived from a 3D field simulation using Agilent's HFSS tool. This model includes the effects of the microstrip-to-coplanar transition, the air gap coplanar crossover, and the coplanar-to-microstrip transition. The S-Parameters are imported directly into the MWO model using an S2P file format.

The Stratedge LCC transition is the next element. That model is presented in Figure 3, and contains the appropriate substrate materials and transition elements. Bond wire transitions connect the LLC transition to a ceramic microstrip line that routes the RF to the device. The output side employs the same model, with the elements placed in reverse order.

A 3D view of the model is presented in Figure 4. Note that the device is mounted near the output side of the Stratedge inner gap area tom minimize losses on the output.

Figure 2: Inner Block Model

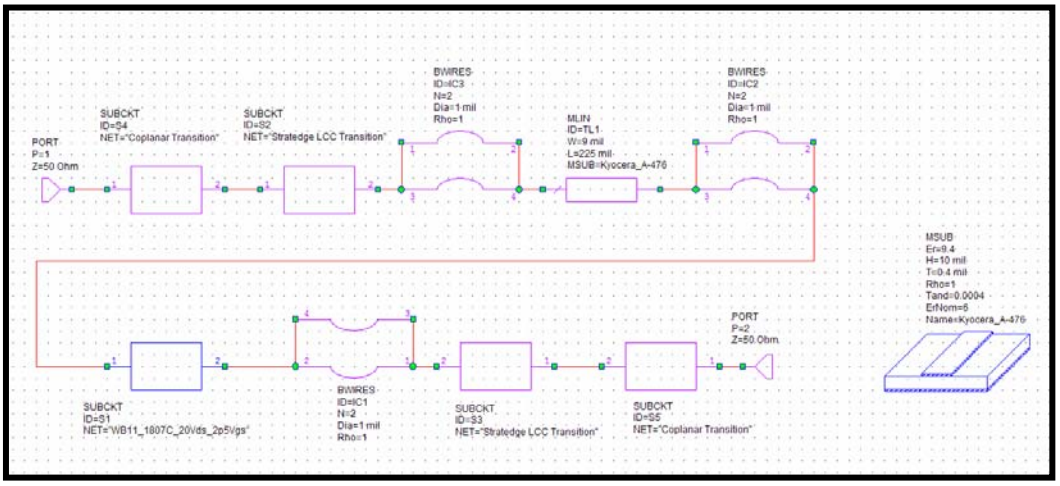


Figure 3: Stratedge LCC Transition Model

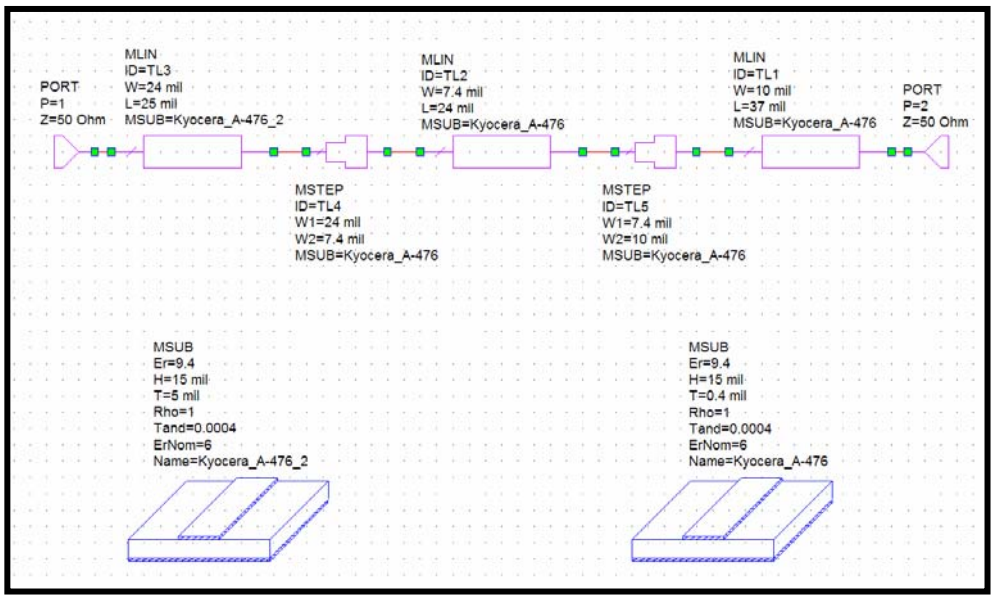
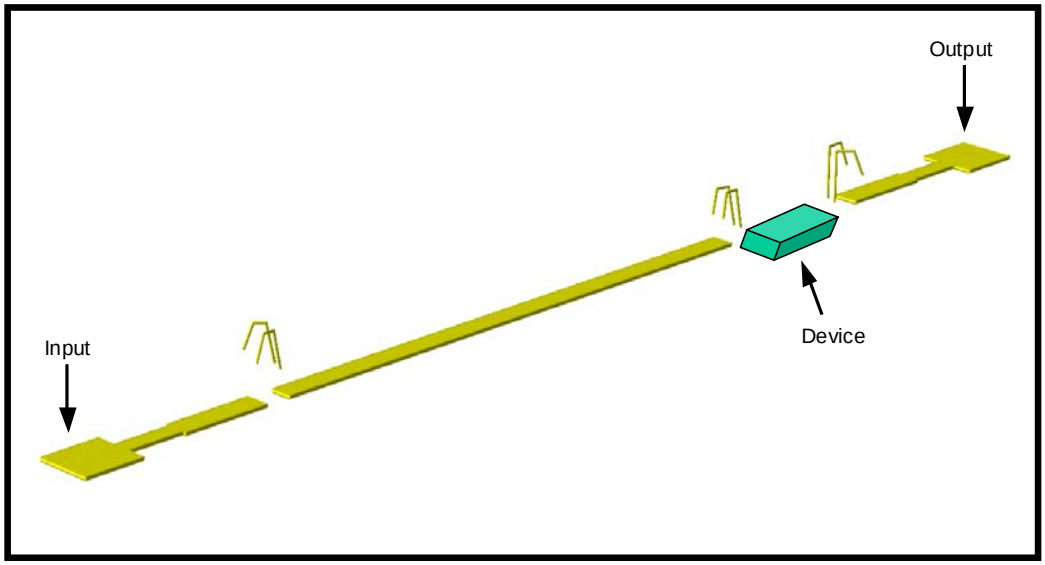


Figure 4: 3-DTransition View



Given this model, a matching circuit may be designed on the output side that presents the proper gamma load to the device. The model of Figure 5 provides a simple approach to design the proper distributed elements. An input port, with impedance equal to the conjugate of gamma load represents the device output. The output transition model is inserted and the resulting output impedance is matched to 50 using standard Smith Chart matching techniques. In this example, a capacitive open stub provided nice match (see Figure 6).

Figure 5: Output Gamma Load Match Model

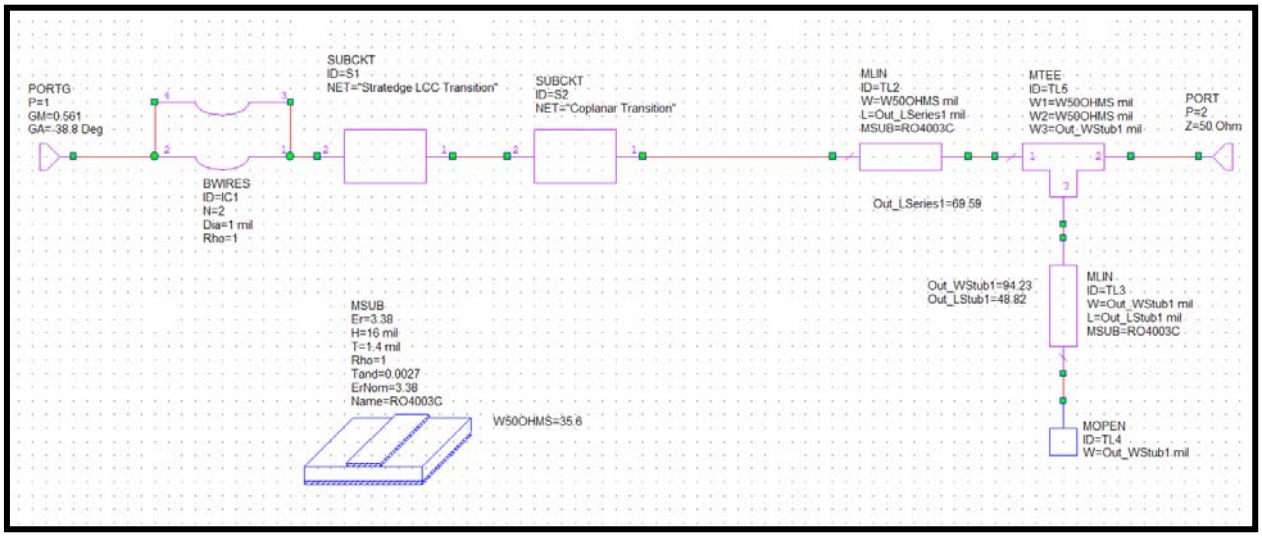
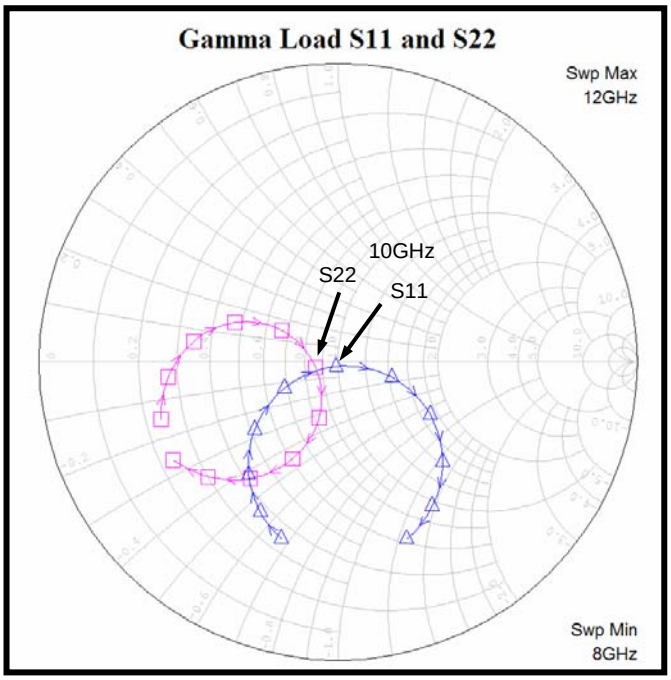


Figure 6: Output Gamma Load Match Performance



4.3 Step 3 – Design for Stability

The next step is to assure unconditional stability. Given the output matching structure defined in the previous step, we can add the input transition circuit and analyze the stability circles. Then we can try different topologies to stabilize the circuit.

The circuit so far looks like the model of Figure 7. The stability analysis must be analyzed over the full bandwidth of 45MHz to 20GHz to guarantee that no oscillations will occur. The input and output stability circle results, without stabilization, are presented in Figure 8. Note that because of the phase extension caused by the transition circuits, the circles completely encompass the center, making loss-less stabilization very difficult; hence, resistive stabilization is utilized. Since we are working with a power amplifier, it is preferable to place the stabilizing resistors on the input. Series resistive elements will push the circles toward the outer part of the Smith chart in the low impedance region, and shunt resistive elements will push the circles toward the outside in the high impedance part of the chart. Employing both series and shunt elements will force the circles out around the entire region.

For this example the stabilization circuit presented in Figure 9 provides the best performance. Starting on the device side, this model employs a series resistor, followed by a shunt resistor. The keep the shunt resistor from affecting DC bias, a series capacitor provides blocking. The resistors for this circuit were chosen to be 0805 case size, but 0402 could be used for higher frequency performance. Since there is no library element for the 0805 chip resistor, the pseudo-distributed model of Figure 10 was used, with different resistor values used for the two components.

Figure 7: Stability Circles Circuit

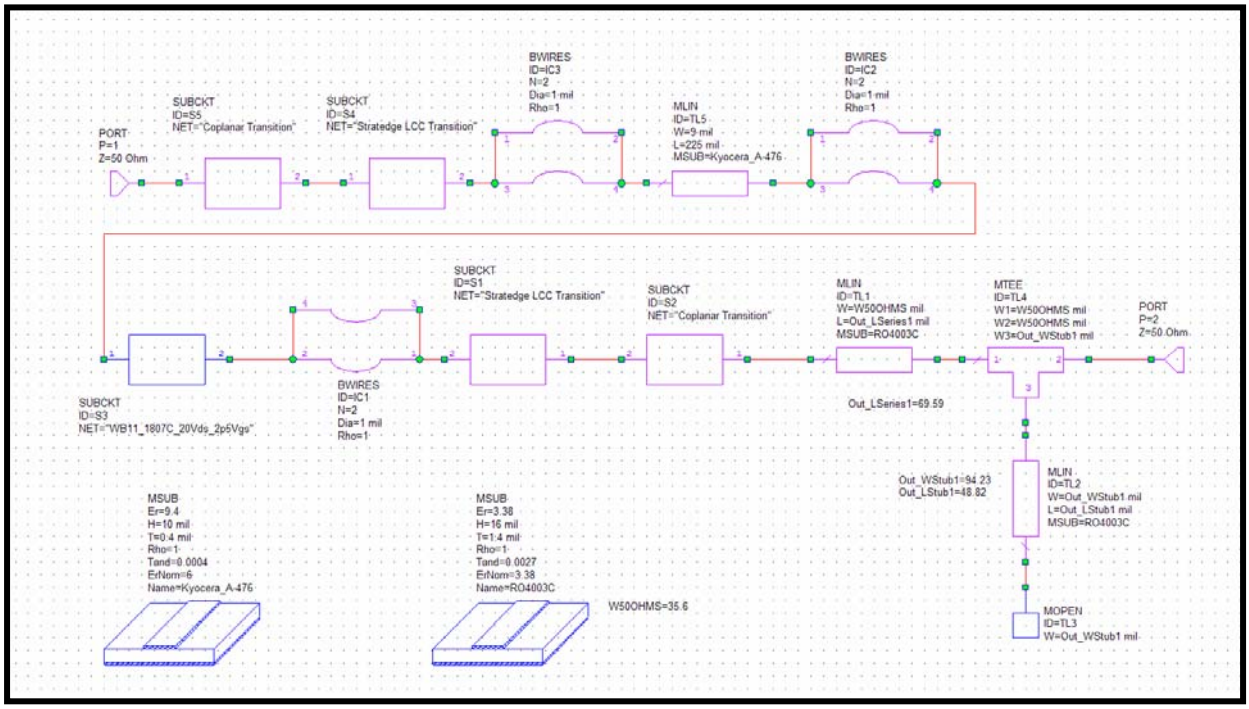


Figure 8: Stability Circles

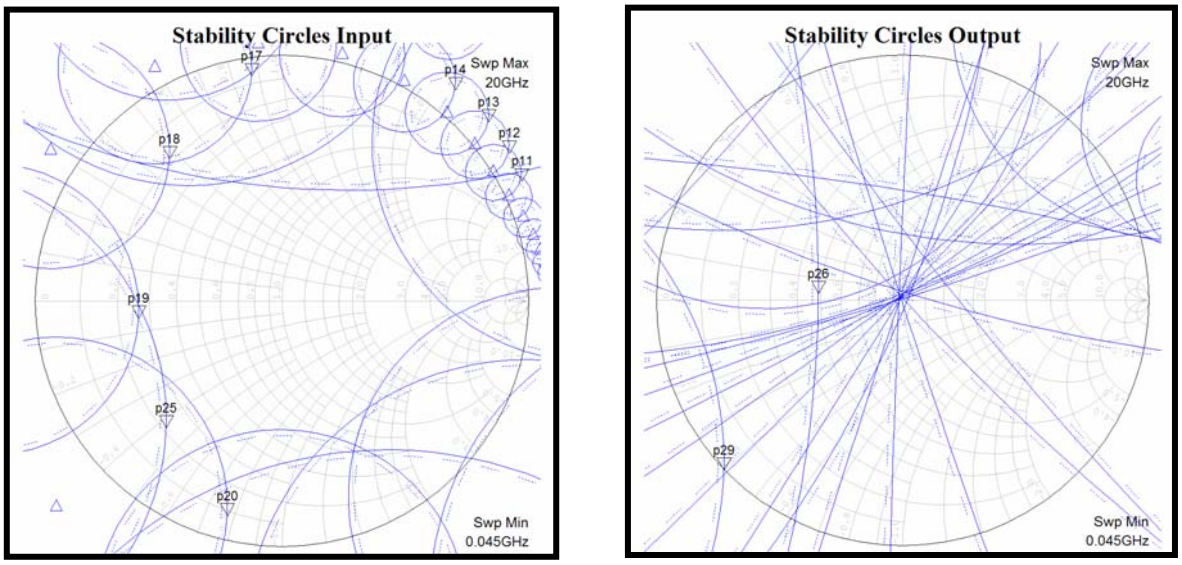


Figure 9: Stabilization Circuit

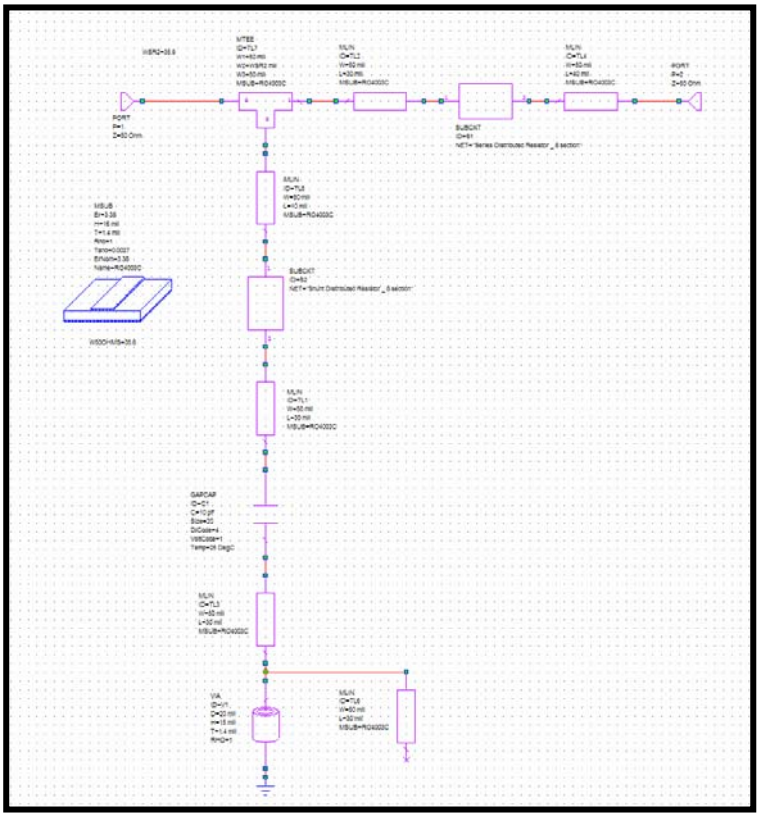


Figure 10: 0805 Resistor Model

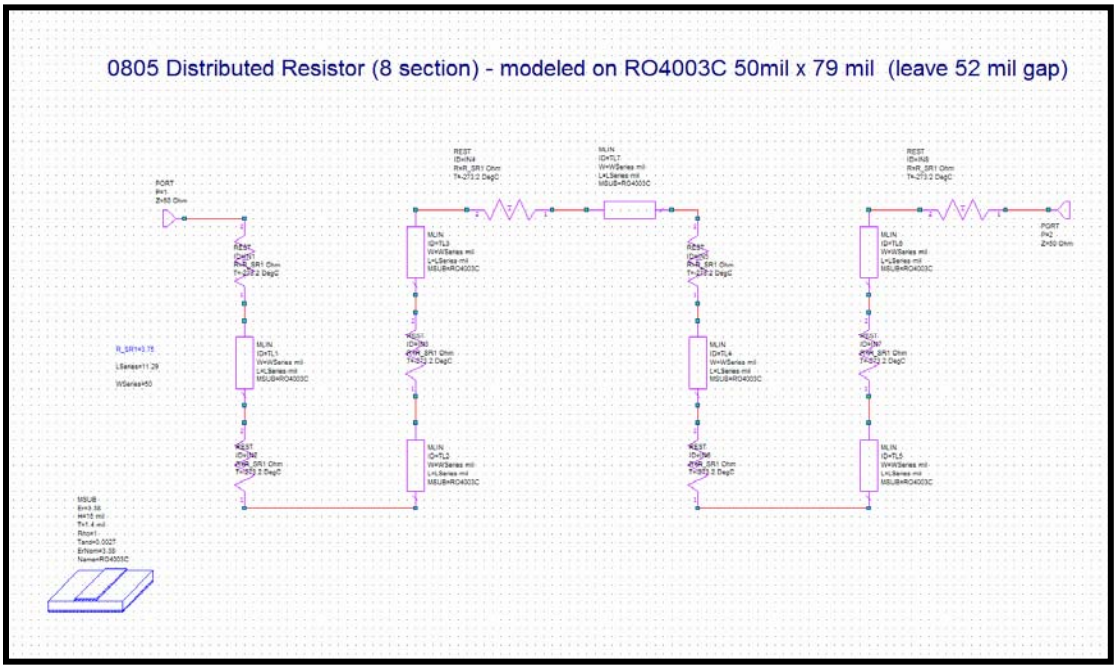


Figure 11 shows the resultant stability circle performance with the stabilizing elements included. There is a small area that intersects the positive resistance region of the Smith Chart, but with the additional loss of the remaining elements that will need to be added to complete the circuits, these points should be completely excluded from the possible impedance regime.

Evidently, adding lossy elements in the matching structure causes a loss of performance. Figure 12 shows that the available gain after adding the stabilization resistors suffers about a 4-dB decrease. This is an acceptable amount of loss, given the assurance of stabilization. Further, in the context of the life test paradigm it is relative change that is important. Finally, the additional circuit loss may be calibrated out of the measured performance, virtually eliminating the additional loss.

Figure 11: Stabilized Circuit Performance

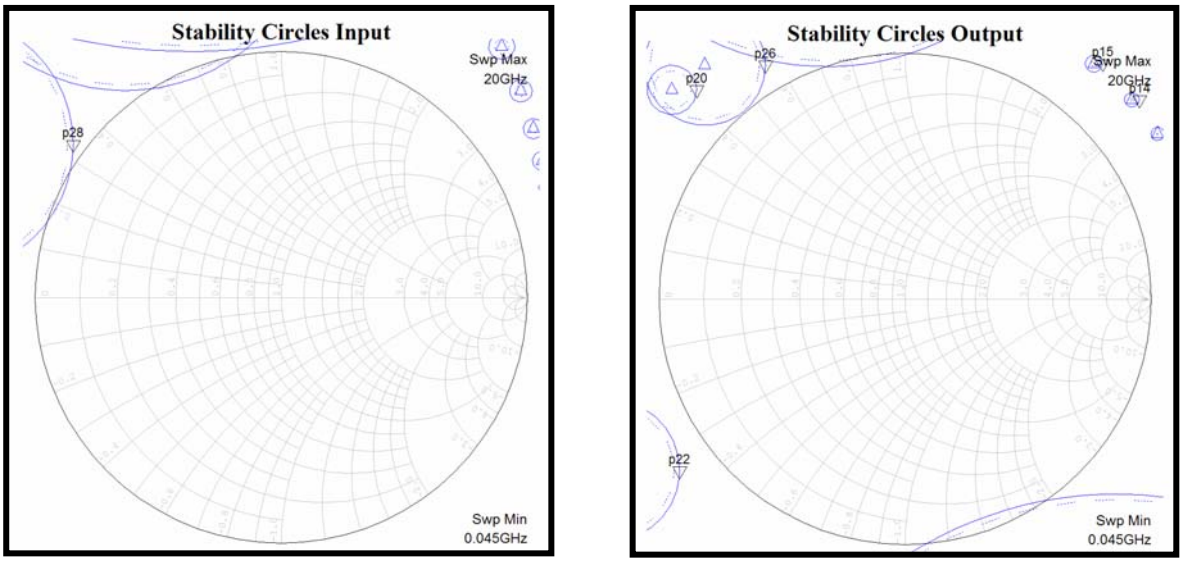
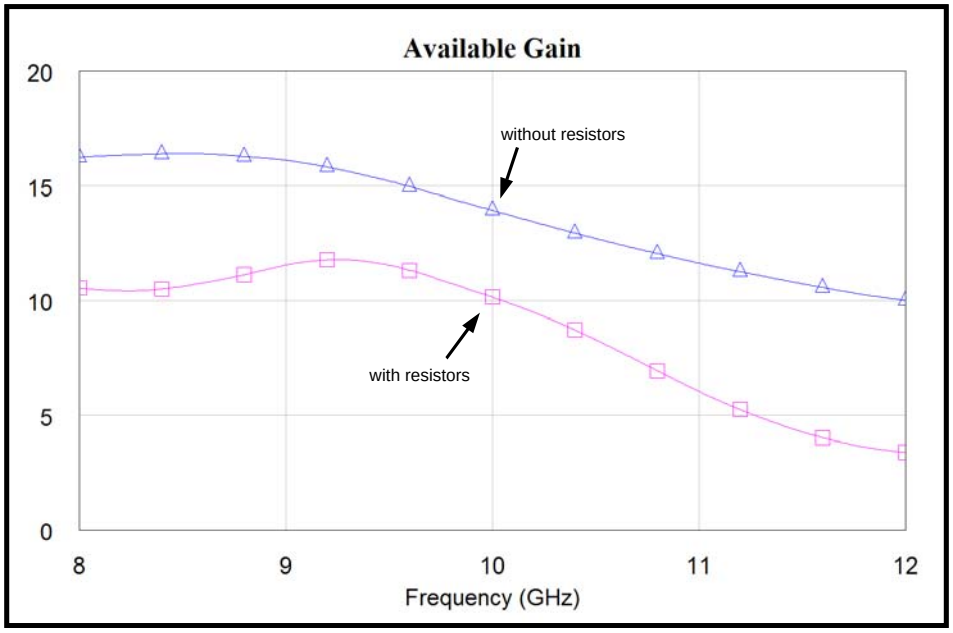


Figure 12: Available Gain Degradation



4.4 Step 4 – Design for Conjugate Match

Now that stability has been achieved while simultaneously providing the desired gamma load on the output, the input may be conjugately matched to maximize gain and return loss. The double-stub circuit of Figure 13 provides a nice match for the input circuit. The input and output return loss performance of the combined circuits are shown in Figure 14. The gain performance is shown in Figure 15.

Figure 13: Input Conjugate Match Circuit

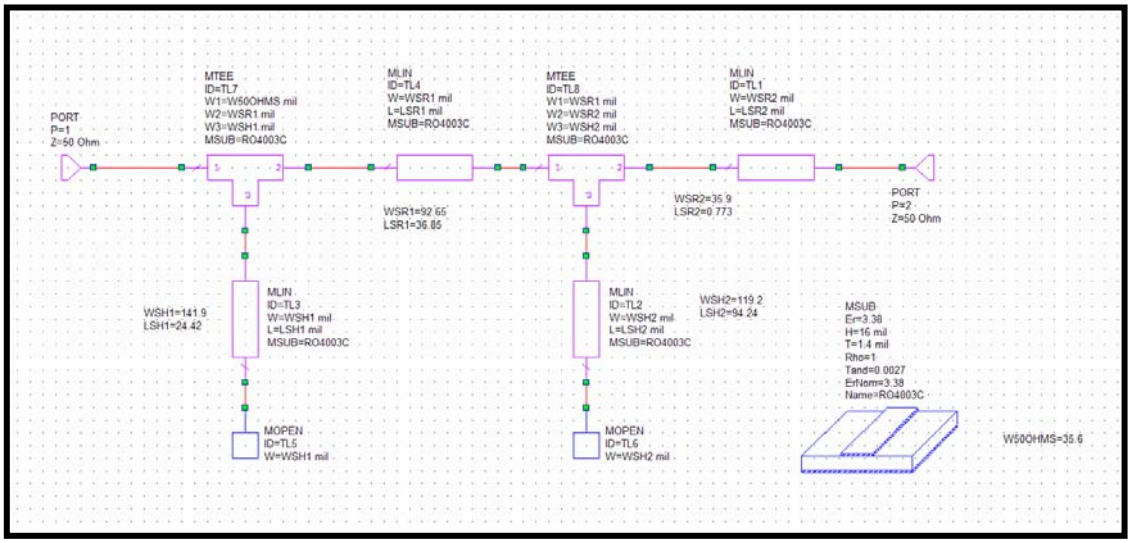


Figure 14: Input and Output Return Loss

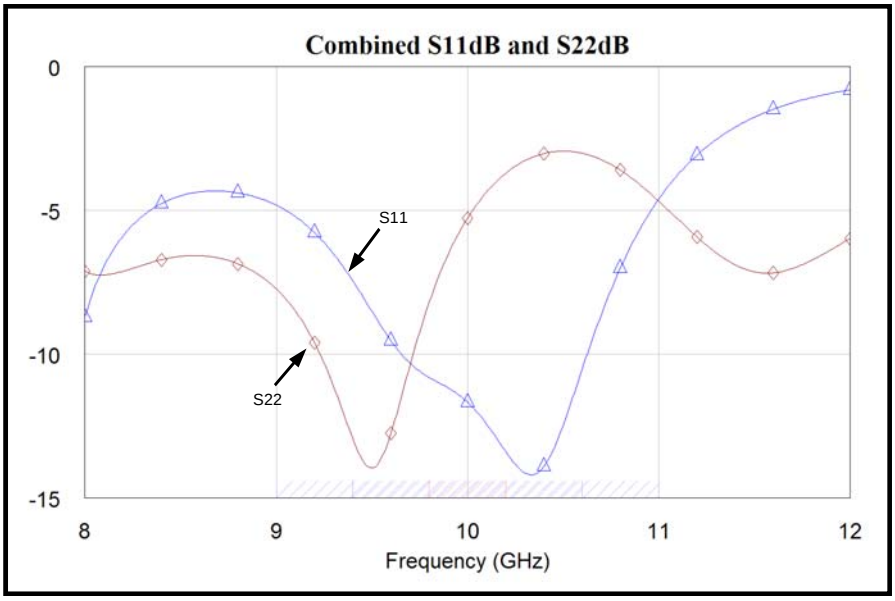
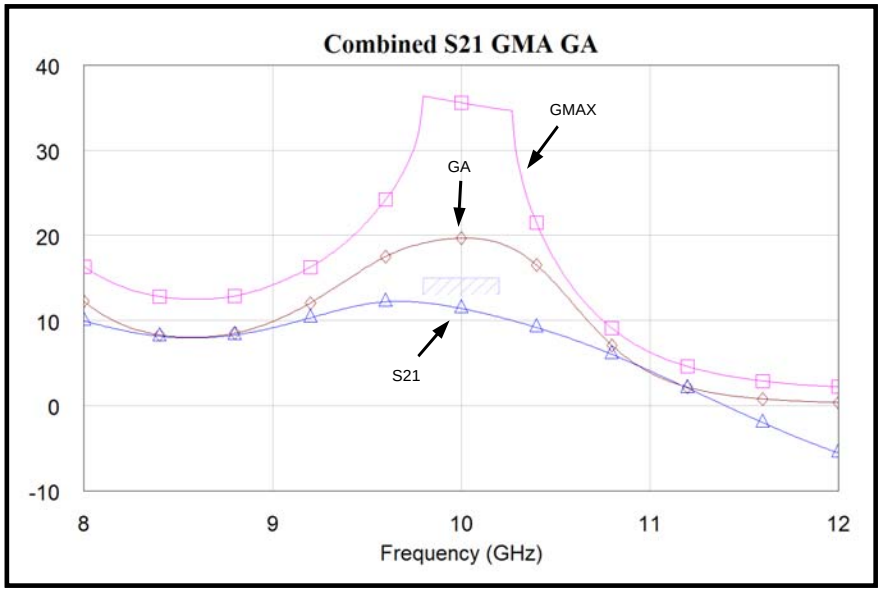


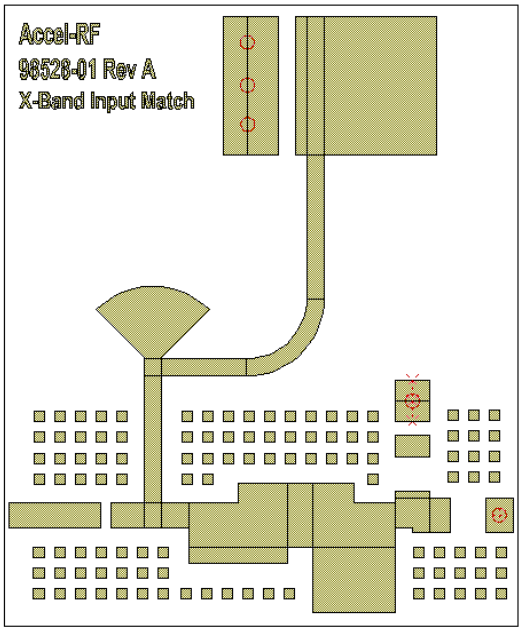
Figure 15: Gain Performance

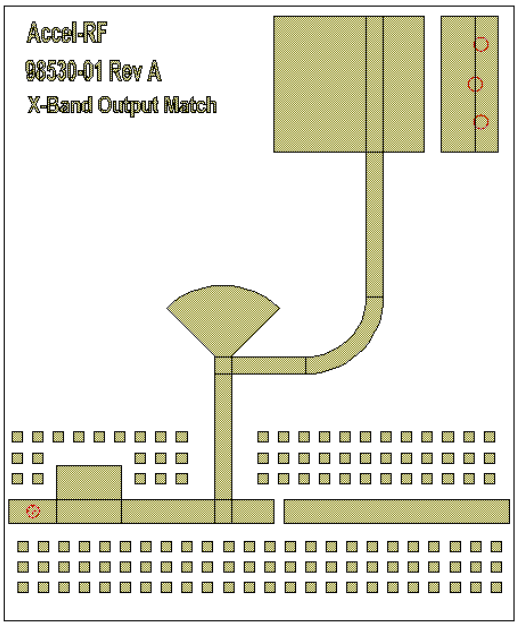


4.5 Step 5 – Add Bias Circuits

The final design step is to add in the required biasing circuits. In this case, quarter-wave chokes worked nicely to maintain good RF performance. The input and output RF lines carry the bias to the device gate and drain ports. The final input and output circuit layouts are shown in Figure 16.

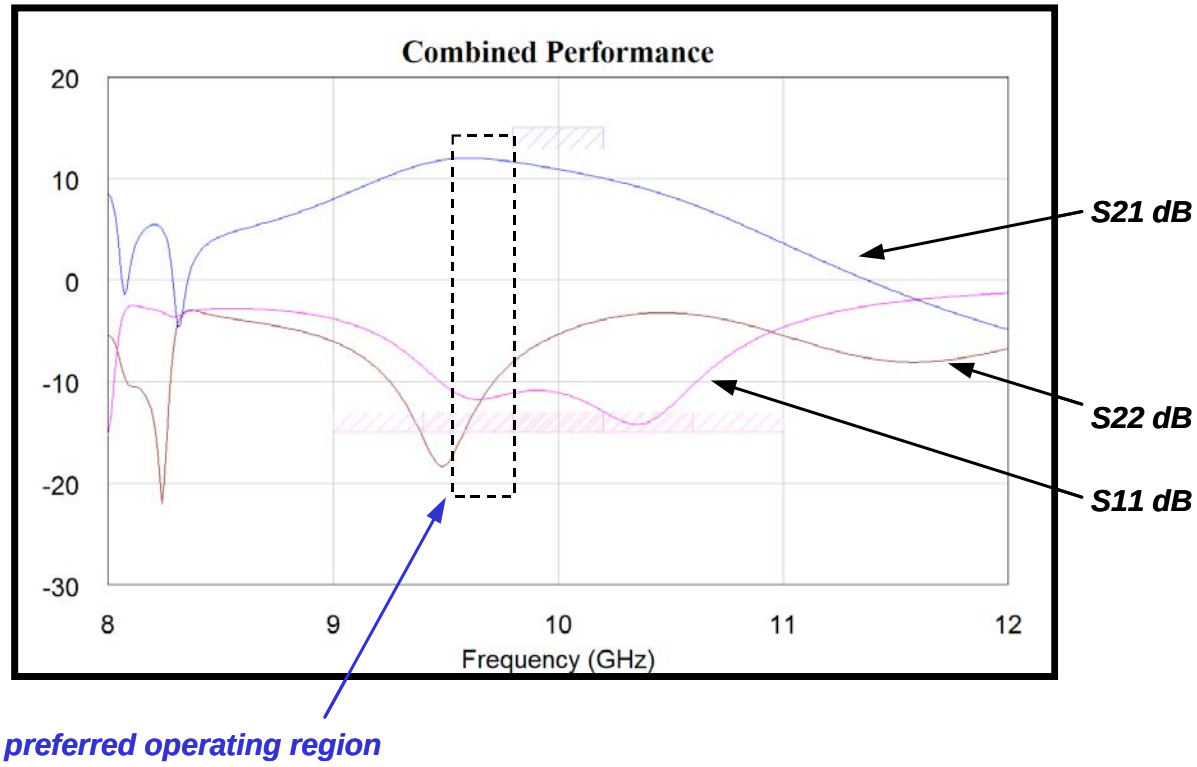
Figure 16: Input / Output Matching Circuits





The overall performance of the combined matching circuits is presented in Figure 17. In order to optimize input and output return loss performance, peak gain, and gamma load performance, the operating frequency has been shifted down by about 0.3GHz. This was considered a reasonable tradeoff between circuit performance, desired operating frequency, and test set performance.

Figure 17: Overall Performance



Tabular results of the overall circuit is presented in Figure 18. The stability factors show unconditional stability, gamma load is very close to the optimal value, the circuit has reasonable gain, and the input/output return loss are >10dB at the recommended operating frequency.

The next phase of the process is to verify model integrity and estimate the input and output loss factors to be used in the RF calibration process.

Figure 18: Stability Performance

Frequency (GHz)	K() Combined	B1() Combined	|S(1,1)| Device Output Load	Ang(S(1,1)) (Deg) Device Output Load	DB(|S(2,1)|) Combined	DB(|S(1,1)|) Combined	DB(|S(2,2)|) Combined
9	1.9467	0.92975	0.62778	74.012	7.769	-4.5154	-6.1794
9.05	1.909	0.93848	0.62571	71.972	8.1749	-4.9056	-6.7259
9.1	1.8731	0.94621	0.62372	69.977	8.5749	-5.3736	-7.3843
9.15	1.838	0.95279	0.62149	68.023	8.9685	-5.9345	-8.1897
9.2	1.7999	0.95736	0.61929	66.106	9.3562	-6.5987	-9.174
9.25	1.7622	0.95987	0.61681	64.224	9.7232	-7.388	-10.4
9.3	1.7209	0.95943	0.61434	62.372	10.07	-8.3125	-11.93
9.35	1.6801	0.95633	0.61156	60.55	10.38	-9.3968	-13.897
9.4	1.6356	0.94947	0.60877	58.754	10.657	-10.629	-16.323
9.45	1.591	0.9392	0.60567	56.985	10.884	-11.985	-18.884
9.5	1.5429	0.92514	0.60254	55.237	11.069	-13.354	-19.69
9.55	1.495	0.90804	0.59909	53.514	11.2	-14.54	-17.708
9.6	1.4481	0.88842	0.59561	51.809	11.282	-15.265	-15.064
9.65	1.4021	0.86677	0.59182	50.126	11.312	-15.356	-12.786
9.7	1.3543	0.84294	0.58799	48.458	11.305	-14.929	-10.946
9.75	1.3089	0.81781	0.58384	46.811	11.256	-14.301	-9.4778
9.8	1.2635	0.79103	0.57967	45.176	11.18	-13.675	-8.2807
9.85	1.2196	0.76355	0.57518	43.56	11.083	-13.173	-7.3147
9.9	1.1776	0.73455	0.57067	41.955	10.969	-12.83	-6.5046
9.95	1.1419	0.70474	0.56585	40.367	10.83	-12.671	-5.8283
10	1.1106	0.67366	0.56101	38.786	10.678	-12.678	-5.2525
10.05	1.0881	0.64233	0.55588	37.221	10.505	-12.86	-4.769
10.1	1.0736	0.61062	0.55073	35.661	10.318	-13.198	-4.3565
10.15	1.0705	0.58015	0.5453	34.115	10.109	-13.675	-4.0152
10.2	1.0771	0.55125	0.53987	32.572	9.8867	-14.231	-3.7314
10.25	1.0977	0.52592	0.53415	31.04	9.6405	-14.791	-3.5078
10.3	1.1303	0.50482	0.52845	29.508	9.3773	-15.189	-3.3347
10.35	1.1796	0.49023	0.52247	27.985	9.0884	-15.254	-3.2184
10.4	1.2429	0.48257	0.51651	26.457	8.7796	-14.85	-3.1491
10.45	1.3244	0.48357	0.51029	24.937	8.4427	-14.031	-3.1313
10.5	1.4213	0.49323	0.50409	23.407	8.085	-12.954	-3.1583
10.55	1.5377	0.51242	0.49764	21.881	7.7002	-11.796	-3.2333
10.6	1.6677	0.54008	0.49122	20.341	7.2991	-10.656	-3.3473
10.65	1.8178	0.5764	0.48456	18.8	6.8738	-9.599	-3.5049
10.7	1.9841	0.61987	0.47792	17.238	6.433	-8.6416	-3.6991
10.75	2.1705	0.66957	0.47103	15.671	5.9732	-7.7888	-3.9298
10.8	2.3724	0.72369	0.46418	14.075	5.5033	-7.0324	-4.1897
10.85	2.6003	0.78149	0.45708	12.469	5.0182	-6.3671	-4.4829
10.9	2.8426	0.84065	0.45	10.824	4.5296	-5.7797	-4.7958
10.95	3.103	0.90003	0.44267	9.1619	4.0343	-5.2624	-5.1255
11	3.3756	0.95839	0.43535	7.4515	3.5405	-4.8053	-5.4652

recommended operating frequency

10GHz Gamma Load Goal = 0.561 ang 38.8

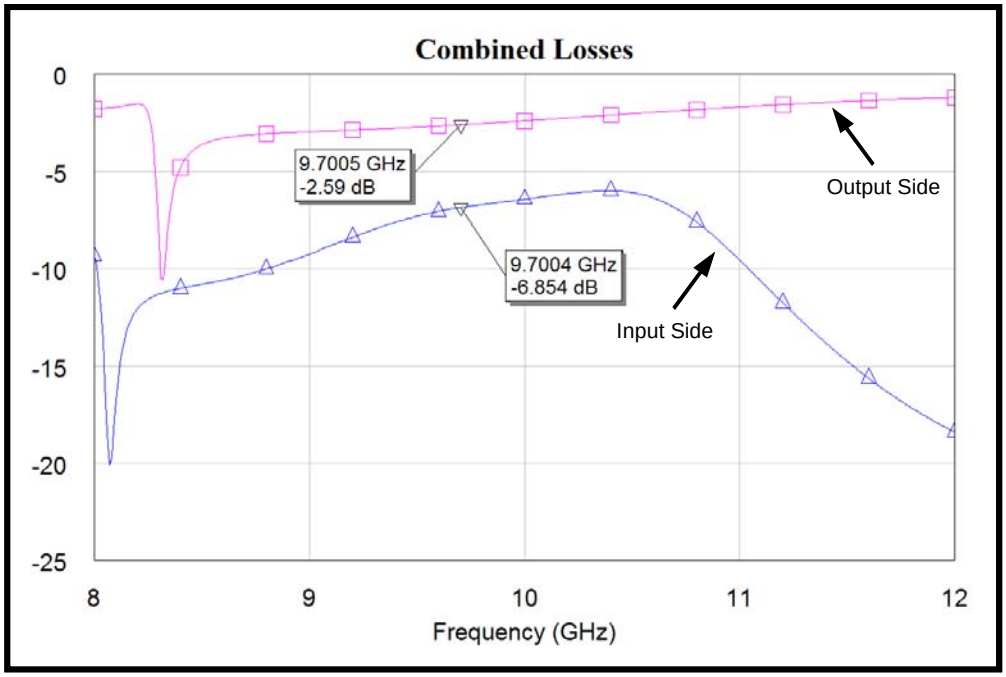
**** K1>1 & B>0 Necessary to Guarantee Unconditional Stability***

4.6 Step 6 – Estimate Input and Output Losses

High-temperature life testing is used to accelerate aging effects in semiconductor devices (e.g. gate sinking). For the reliability engineer, the goal is to maintain a known and constant channel temperature for all devices under test. An important contributor to channel temperature calculations is the amount of power dissipated in the device. DC and RF input signals inject energy into the device, and the RF output power removes energy. To obtain a better estimate of the actual total power dissipation in the device, it is we must be able to reference signals levels to the device.

In the AARTS system, calibration is conveniently performed at the fixture input and output ports. However, the losses between the fixture interface and the device can be significant. The next step is to estimate those losses. First, we break the model into and input and output section and simulate the responses. The results are shown in Figure 19.

Figure 19: Input and Output Losses



As expected, the input loss is higher than the output loss (-6.854dB and –2.59dB, respectively at the preferred operating frequency). These numbers may be employed in the calibration process to obtain a better estimate of the actual device operating points. To better estimate the power actually delivered to and extracted from the device, the model should employ a complex port source, equal to the complex impedance of the device at the operating frequency.

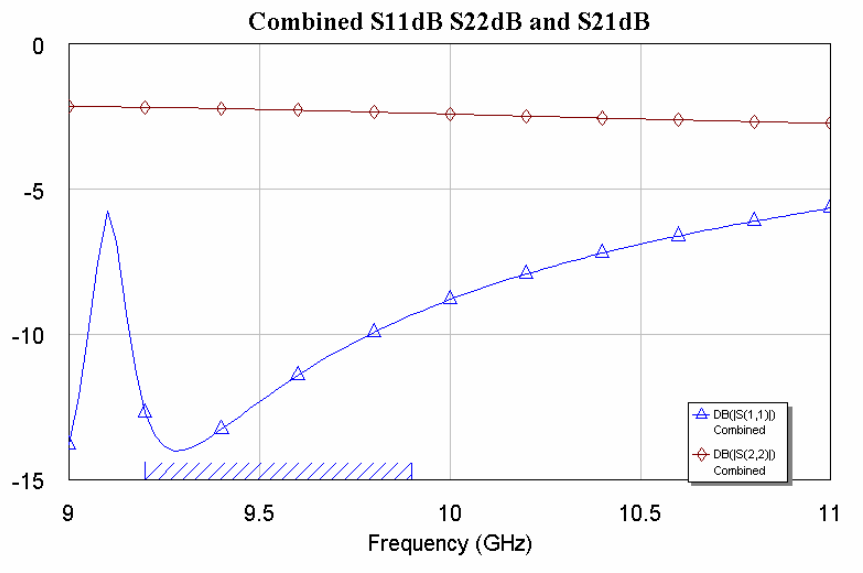
This method provides a very good indication of the relative losses. If, in model verification phase of the process, the overall fixture loss is higher or lower than predicted, this ratio could be applied to further refine the correct calibration factors.

5 Model Verification

The best way to verify model integrity is to compare predicted performance against measured data. A couple of test scenarios were employed to test the model accuracy. First, a center block test carrier plate was created comprising all of the elements that would exist in the actual circuit, but with the actual device replaced by a short piece of 50-Ω transmission line. A second test of replacing the device with 50-Ω shunt resistors to ground provides a useful test of input and output matching integrity.

Figure 20 and Figure 21 show the modeled S-Parameter performance of the circuits with a 50-Ω through. In both cases wideband and narrowband responses are presented.

Figure 20: 50-Ω Through Test (S21)



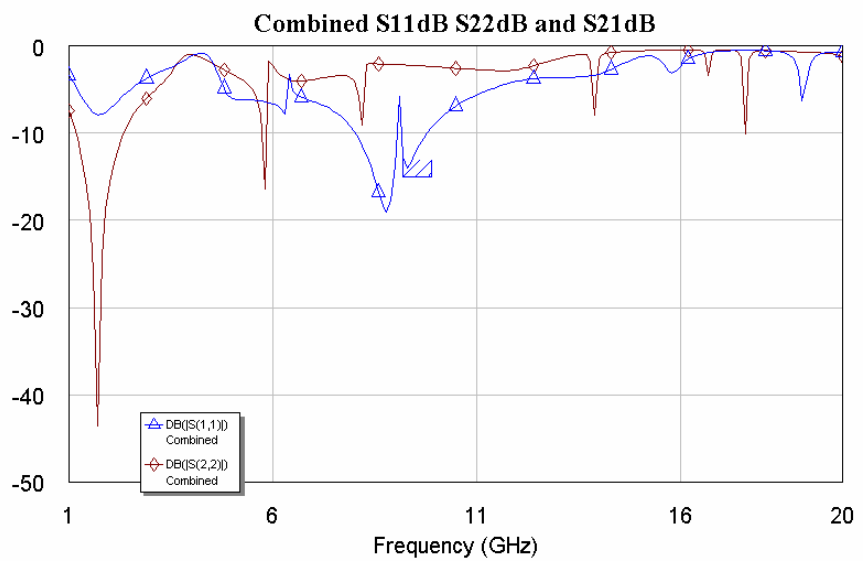


Figure 21: 50-Ω Through Test (S11 & S22)